

# TMS4164 65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

MAY 1985--REVISED NOVEMBER 1985

*This Data Sheet Is Applicable to All TMS4164s Symbolized with Code "A" as Described on Page 4-57.*

- 65,536 X 1 Organization
- Single 5-V Supply (10% Tolerance)
- JEDEC Standardized Pinout in Dual-in-Line Package
- Performance Ranges:

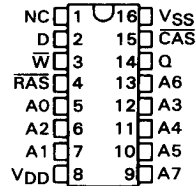
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
'4164-12	120 ns	70 ns	230 ns	255 ns
'4164-15	150 ns	85 ns	260 ns	290 ns
'4164-20	200 ns	135 ns	330 ns	345 ns

- Upward Pin Compatible with TMS4116 (16K Dynamic RAM)
- First Military Version of 64K DRAM
- Also Available with MIL-STD-883B Processing and L(0°C to 70°C), E(-40°C to 85°C), S(-55°C to 100°C), or M(-55°C to 125°C) Temperature Ranges
- Operations of the TMS4164 Can Be Controlled by TI's TMS4500A and/or THCT4501 Dynamic RAM Controllers
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.8% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Common I/O Capability with Early Write Feature
- Page-Mode Operation for Faster Access
- Low Power Dissipation
  - Operating . . . 135 mW (Typ)
  - Standby . . . 17.5 mW (Typ)
- SMOS (Scaled-MOS) N-Channel Technology

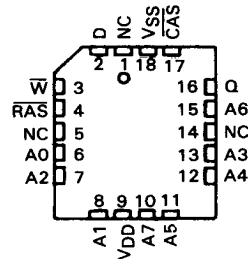
### description

The TMS4164 is a high-speed, 65,536-bit, dynamic random-access memory, organized as 65,536 words of one bit each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

### N PACKAGE (TOP VIEW)



### FP PACKAGE (TOP VIEW)



### PIN NOMENCLATURE

A0-A7	Address Inputs
CAS	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
RAS	Row-Address Strobe
VDD	5-V Supply
VSS	Ground
W	Write Enable

**PRODUCTION DATA** documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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INSTRUMENTS**

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# TMS4164

## 65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

The TMS4164 features  $\overline{\text{RAS}}$  access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation is 135 mW typical operating and 17.5 mW typical standby.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with  $\overline{\text{RAS}}$  in order to retain data.  $\overline{\text{CAS}}$  can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility. Pin 1 has no internal connection to allow compatibility with other 64K RAMs that use this pin for an additional function.

The TMS4164 is offered in 16-pin dual-in-line plastic (N suffix) and 18-lead plastic chip carrier (FP suffix) packages. The dual-in-line plastic package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers. The TMS4164 is guaranteed for operation from 0°C to 70°C.

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### Dynamic RAMs

#### operation

##### address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ( $\overline{\text{RAS}}$ ). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ( $\overline{\text{CAS}}$ ). All addresses must be stable on or before the falling edges of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$ .  $\overline{\text{RAS}}$  is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder.  $\overline{\text{CAS}}$  is used as a chip select activating the column decoder and the input and output buffers.

##### write enable ( $\overline{\text{W}}$ )

The read or write mode is selected through the write-enable ( $\overline{\text{W}}$ ) input. A logic high on the  $\overline{\text{W}}$  input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When  $\overline{\text{W}}$  goes low prior to  $\overline{\text{CAS}}$ , data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

##### data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of  $\overline{\text{CAS}}$  or  $\overline{\text{W}}$  strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle,  $\overline{\text{W}}$  is brought low prior to  $\overline{\text{CAS}}$  and the data is strobed in by  $\overline{\text{CAS}}$  with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle,  $\overline{\text{CAS}}$  will already be low, thus the data will be strobed in by  $\overline{\text{W}}$  with setup and hold times referenced to this signal.

##### data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until  $\overline{\text{CAS}}$  is brought low. In a read cycle the output goes active after the access time interval  $t_a(\text{C})$  that begins with the negative transition of  $\overline{\text{CAS}}$  as long as  $t_a(\text{R})$  is satisfied. The output becomes valid after the access time has elapsed and remains valid while  $\overline{\text{CAS}}$  is low;  $\overline{\text{CAS}}$  going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

##### refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless  $\overline{\text{CAS}}$  is applied, the  $\overline{\text{RAS}}$ -only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with  $\overline{\text{RAS}}$  causes all bits in each row to be refreshed.  $\overline{\text{CAS}}$  can remain high (inactive) for this refresh sequence to conserve power.

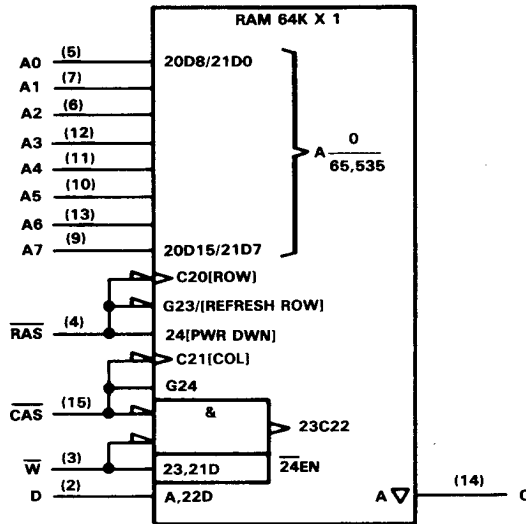
**page mode**

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and  $\overline{\text{RAS}}$  are applied to multiple 64K RAMs.  $\overline{\text{CAS}}$  is then decoded to select the proper RAM.

**power up**

After power up, the power supply must remain at its steady-state value for 1 ms. In addition,  $\overline{\text{RAS}}$  must remain high for 100  $\mu\text{s}$  immediately prior to initialization. Initialization consists of performing eight  $\overline{\text{RAS}}$  cycles before proper device operation is achieved.

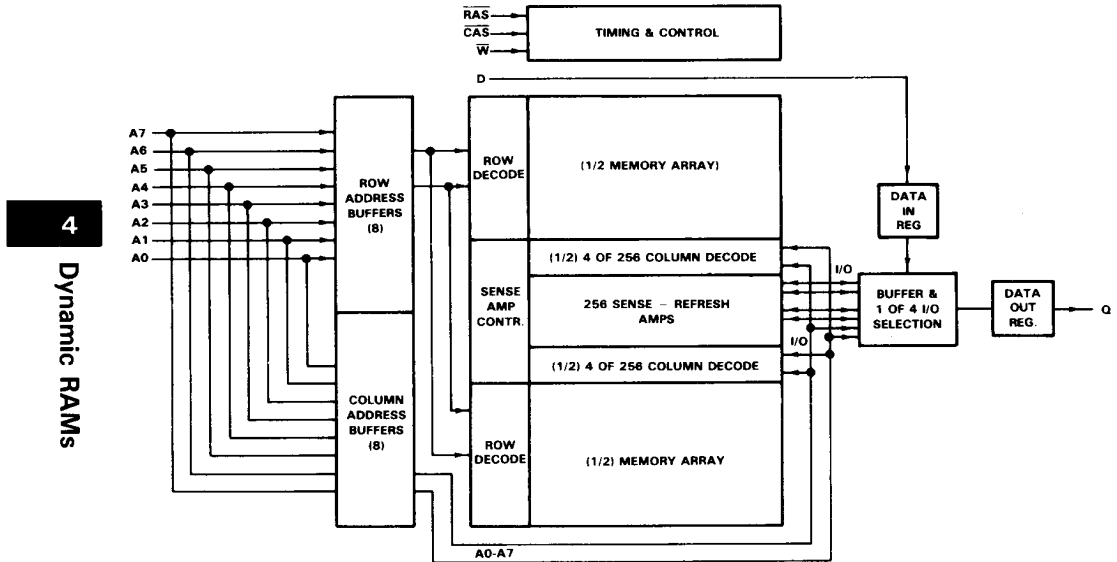
**logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the dual-in-line package.

**TMS4164**  
**65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY**

functional block diagram



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**Dynamic RAMs**

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted) †**

Voltage on any pin except V <sub>DD</sub> and data out (see Note 1)	-1.5 V to 10 V
Voltage on V <sub>DD</sub> supply and data out with respect to V <sub>SS</sub>	-1 V to 6 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to V<sub>SS</sub>.

2. Additional information concerning the handling of ESD sensitive devices is available in a document entitled "Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies" in Section 12.

**recommended operating conditions**

		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Supply voltage	4.5	5	5.5	V
V <sub>SS</sub>	Supply voltage	0			V
V <sub>IH</sub>		V <sub>DD</sub> = 4.5 V		4.8	V
		V <sub>DD</sub> = 5.5 V		6	
V <sub>IL</sub>	Low-level input voltage (see Notes 3 and 4)	-0.6	0.8		V
T <sub>A</sub>	Operating free-air temperature	0	70		°C

- NOTES: 3. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.  
 4. Due to input protection circuitry, the applied voltage may begin to clamp at -0.6 V. Test conditions must comprehend this occurrence. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

**electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	TMS4164-12			TMS4164-15			UNIT	
		MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX		
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -5 mA			2.4				V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4.2 mA				0.4			V
I <sub>I</sub>	Input current (leakage)	V <sub>I</sub> = 0 V to 5.8 V, V <sub>DD</sub> = 5 V, All other pins = 0 V			± 10		± 10		µA
I <sub>O</sub>	Output current (leakage)	V <sub>O</sub> = 0.4 to 5.5 V, V <sub>DD</sub> = 5 V, CAS high			± 10		± 10		µA
I <sub>DD1</sub> <sup>‡</sup>	Average operating current during read or write cycle	t <sub>c</sub> = minimum cycle, All outputs open			40	48	35	45	mA
I <sub>DD2</sub> <sup>§</sup>	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open			3.5	5	3.5	5	mA
I <sub>DD3</sub> <sup>‡</sup>	Average refresh current	t <sub>c</sub> = minimum cycle, CAS high and RAS cycling, All outputs open			28	40	25	37	mA
I <sub>DD4</sub>	Average page-mode current	t <sub>c(P)</sub> = minimum cycle, RAS low and CAS cycling, All outputs open			28	40	25	37	mA

<sup>†</sup>All typical values are at T<sub>A</sub> = 25 °C and nominal supply voltages.

<sup>‡</sup>Additional information on page 4-58.

<sup>§</sup>V<sub>IL</sub> > -0.6V. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

**TMS4164**  
**65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY**

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TMS4164-20			UNIT
		MIN	TYP†	MAX	
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -5 mA			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4.2 mA			V
I <sub>I</sub>	Input current (leakage)	V <sub>I</sub> = 0 V to 5.8 V, V <sub>DD</sub> = 5 V All other pins = 0 V			±10 μA
I <sub>O</sub>	Output current (leakage)	V <sub>O</sub> = 0.4 to 5.5 V, V <sub>DD</sub> = 5 V, CAS high			±10 μA
I <sub>DD1</sub> ‡	Average operating current during read or write cycle	t <sub>c</sub> = minimum cycle All outputs open			27 37 mA
I <sub>DD2</sub> §	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open			3.5 5 mA
I <sub>DD3</sub> ‡	Average refresh current	t <sub>c</sub> = minimum cycle, CAS high and RAS cycling, All outputs open			20 32 mA
I <sub>DD4</sub>	Average page-mode current	t <sub>c</sub> (P) = minimum cycle, RAS low and CAS cycling, All outputs open			20 32 mA

† All typical values are at T<sub>A</sub> = 25°C and nominal supply voltages.

‡ Additional information on page 4-58.

§ V<sub>IL</sub> > -0.6V. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

capacitance over recommended supply voltage range and operating free-air temperature range,  
f = 1 MHz

PARAMETER	TYP†	MAX	UNIT
C <sub>i(A)</sub>	4	5	pF
C <sub>i(D)</sub>	4	5	pF
C <sub>i(RC)</sub>	6	8	pF
C <sub>i(W)</sub>	6	8	pF
C <sub>o</sub>	5	6	pF

† All typical values are at T<sub>A</sub> = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER	TEST CONDITIONS	ALT. SYMBOL	TMS4164-12		TMS4164-15		UNIT
			MIN	MAX	MIN	MAX	
t <sub>A(C)</sub>	C <sub>L</sub> = 100 pF, Load = 2 Series 74 TTL gates	t <sub>CAC</sub>	70		85		ns
t <sub>a(R)</sub>	C <sub>L</sub> = 100 pF, t <sub>RLCL</sub> = MAX, Load = 2 Series 74 TTL gates	t <sub>RAC</sub>	120		150		ns
t <sub>dis(CH)</sub>	C <sub>L</sub> = 100 pF, Load = 2 Series 74 TTL gates	t <sub>OFF</sub>	0	40	0	40	ns

**switching characteristics over recommended supply voltage range and operating free-air temperature range**

PARAMETER	TEST CONDITIONS	ALT. SYMBOL	TMS4164-20		UNIT
			MIN	MAX	
$t_{a(C)}$ Access time from $\overline{CAS}$	$C_L = 100$ pF, Load = 2 Series 74 TTL gates	$t_{CAC}$		135	ns
$t_{a(R)}$ Access time from $\overline{RAS}$	$C_L = 100$ pF, $t_{RLCL} = \text{MAX}$ , Load = 2 Series 74 TTL gates	$t_{RAC}$		200	ns
$t_{dis(CH)}$ Output disable time after $\overline{CAS}$ high	$C_L = 100$ pF, Load = 2 Series 74 TTL gates	$t_{OFF}$	0	50	ns

**TMS4164**  
**65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY**

timing requirements over recommended supply voltage range and operating free-air temperature range (see Note 1)

**4**  
**Dynamic RAMS**

	ALT. SYMBOL	TMS4164-12		TMS4164-15		UNIT
		MIN	MAX	MIN	MAX	
t <sub>c(P)</sub> Page-mode cycle time	t <sub>PC</sub>	130		145		ns
t <sub>c(rd)</sub> Read cycle time <sup>†</sup>	t <sub>RC</sub>	230		260		ns
t <sub>c(W)</sub> Write cycle time	t <sub>WC</sub>	230		260		ns
t <sub>c(rdW)</sub> Read-write/read-modify-write cycle time	t <sub>RWC</sub>	255		290		ns
t <sub>w(CH)</sub> Pulse duration, $\overline{\text{CAS}}$ high (precharge time) <sup>‡</sup>	t <sub>CP</sub>	50		50		ns
t <sub>w(CL)</sub> Pulse duration, $\overline{\text{CAS}}$ low <sup>§</sup>	t <sub>CAS</sub>	70	10,000	85	10,000	ns
t <sub>w(RH)</sub> Pulse duration, $\overline{\text{RAS}}$ high (precharge time)	t <sub>RP</sub>	80		100		ns
t <sub>w(RL)</sub> Pulse duration, $\overline{\text{RAS}}$ low <sup>¶</sup>	t <sub>RAS</sub>	120	10,000	150	10,000	ns
t <sub>w(W)</sub> Write pulse duration	t <sub>WP</sub>	40		45		ns
t <sub>t</sub> Transition times (rise and fall) for $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$	t <sub>T</sub>	3	50	3	50	ns
t <sub>su(CA)</sub> Column-address setup time	t <sub>ASC</sub>	-5		-5		ns
t <sub>su(RA)</sub> Row-address setup time	t <sub>ASR</sub>	0		0		ns
t <sub>su(D)</sub> Data setup time	t <sub>DS</sub>	0		0		ns
t <sub>su(rd)</sub> Read-command setup time	t <sub>RCS</sub>	0		0		ns
t <sub>su(WCH)</sub> Write-command setup time before $\overline{\text{CAS}}$ high	t <sub>CWL</sub>	50		50		ns
t <sub>su(WRH)</sub> Write-command setup time before $\overline{\text{RAS}}$ high	t <sub>RWL</sub>	50		50		ns
t <sub>h(CLCA)</sub> Column-address hold time after $\overline{\text{CAS}}$ low	t <sub>CAH</sub>	40		45		ns
t <sub>h(RA)</sub> Row-address hold time	t <sub>RAH</sub>	15		20		ns
t <sub>h(RLCA)</sub> Column-address hold time after $\overline{\text{RAS}}$ low	t <sub>AR</sub>	85		95		ns
t <sub>h(CLD)</sub> Data hold time after $\overline{\text{CAS}}$ low	t <sub>DHC</sub>	40		45		ns
t <sub>h(RLD)</sub> Data hold time after $\overline{\text{RAS}}$ low	t <sub>DHR</sub>	85		95		ns
t <sub>h(WLD)</sub> Data hold time after $\overline{\text{W}}$ low	t <sub>DHW</sub>	40		45		ns
t <sub>h(CHrd)</sub> Read-command hold time after $\overline{\text{CAS}}$ high	t <sub>RCH</sub>	0		0		ns
t <sub>h(RHrd)</sub> Read-command hold time after $\overline{\text{RAS}}$ high	t <sub>RRH</sub>	5		5		ns
t <sub>h(CLW)</sub> Write-command hold time after $\overline{\text{CAS}}$ low	t <sub>WCH</sub>	40		45		ns
t <sub>h(RLW)</sub> Write-command hold time after $\overline{\text{RAS}}$ low	t <sub>WCR</sub>	85		95		ns
t <sub>RLCH</sub> Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high	t <sub>CSH</sub>	120		150		ns
t <sub>CHRL</sub> Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	t <sub>CRP</sub>	0		0		ns
t <sub>CLRH</sub> Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ high	t <sub>RSH</sub>	70		85		ns
t <sub>CLWL</sub> Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{W}}$ low (read-modify-write cycle only)	t <sub>CWD</sub>	40		60		ns
t <sub>RLCL</sub> Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (maximum value specified only to guarantee access time)	t <sub>RCd</sub>	15	50	20	65	ns
t <sub>RLWL</sub> Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{W}}$ low (read-modify-write cycle only)	t <sub>RWD</sub>	110		120		ns
t <sub>WLCL</sub> Delay time, $\overline{\text{W}}$ low to $\overline{\text{CAS}}$ low (early write cycle)	t <sub>WCS</sub>	-5		-5		ns
t <sub>rf</sub> Refresh time interval	t <sub>REF</sub>		4		4	ms

NOTE 1: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V<sub>IL</sub> max and V<sub>IH</sub> min must be met at the 10% and 90% points.

<sup>†</sup> All cycle times assume t<sub>t</sub> = 5 ns.

<sup>‡</sup> Page mode only.

<sup>§</sup> In a read-modify-write cycle, t<sub>CLWL</sub> and t<sub>su(WCH)</sub> must be observed. Depending on the user's transition times, this may require additional  $\overline{\text{CAS}}$  low time (t<sub>w(CL)</sub>). This applies to page-mode read-modify-write also.

<sup>¶</sup> In a read-modify-write cycle, t<sub>RLWL</sub> and t<sub>su(WRH)</sub> must be observed. Depending on the user's transition times, this may require additional  $\overline{\text{RAS}}$  low time (t<sub>w(RL)</sub>).



**timing requirements over recommended supply voltage range and operating free-air temperature range (see Note 1)**

	ALT. SYMBOL	TMS4164-20		UNIT
		MIN	MAX	
$t_c(P)$ Page-mode cycle time	$t_{PC}$	225		ns
$t_c(rd)$ Read cycle time <sup>†</sup>	$t_{RC}$	330		ns
$t_c(W)$ Write cycle time	$t_{WC}$	330		ns
$t_c(rdW)$ Read-write/read-modify-write cycle time	$t_{RWC}$	345		ns
$t_w(CH)$ Pulse duration, $\overline{CAS}$ high (precharge time) <sup>‡</sup>	$t_{CP}$	80		ns
$t_w(CL)$ Pulse duration, $\overline{CAS}$ low <sup>§</sup>	$t_{CAS}$	135	10,000	ns
$t_w(RH)$ Pulse duration, $\overline{RAS}$ high (precharge time)	$t_{RP}$	120		ns
$t_w(RL)$ Pulse duration, $\overline{RAS}$ low <sup>¶</sup>	$t_{RAS}$	200	10,000	ns
$t_w(W)$ Write pulse duration	$t_{WP}$	55		ns
$t_t$ Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	$t_T$	3	50	ns
$t_{su}(CA)$ Column-address setup time	$t_{ASC}$	-5		ns
$t_{su}(RA)$ Row-address setup time	$t_{ASR}$	0		ns
$t_{su}(D)$ Data setup time	$t_{DS}$	0		ns
$t_{su}(rd)$ Read-command setup time	$t_{RCS}$	0		ns
$t_{su}(WCH)$ Write-command setup time before $\overline{CAS}$ high	$t_{CWL}$	60		ns
$t_{su}(WRH)$ Write-command setup time before $\overline{RAS}$ high	$t_{RWL}$	60		ns
$t_h(CLCA)$ Column-address hold time after $\overline{CAS}$ low	$t_{CAH}$	55		ns
$t_h(RA)$ Row-address hold time	$t_{RAH}$	25		ns
$t_h(RLCA)$ Column-address hold time after $\overline{RAS}$ low	$t_{AR}$	120		ns
$t_h(CLD)$ Data hold time after $\overline{CAS}$ low	$t_{DHC}$	55		ns
$t_h(RLD)$ Data hold time after $\overline{RAS}$ low	$t_{DHR}$	145		ns
$t_h(WLD)$ Data hold time after $\overline{W}$ low	$t_{DHW}$	55		ns
$t_h(CHrd)$ Read-command hold time after $\overline{CAS}$ high	$t_{RCH}$	0		ns
$t_h(RHrd)$ Read-command hold time after $\overline{RAS}$ high	$t_{RRH}$	5		ns
$t_h(CLW)$ Write-command hold time after $\overline{CAS}$ low	$t_{WCH}$	55		ns
$t_h(RLW)$ Write-command hold time after $\overline{RAS}$ low	$t_{WCR}$	145		ns
$t_{RLCH}$ Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	$t_{CSh}$	200		ns
$t_{CHRL}$ Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	$t_{CRP}$	0		ns
$t_{CLRH}$ Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	$t_{RSh}$	135		ns
$t_{CLWL}$ Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	$t_{CWD}$	65		ns
$t_{RLCL}$ Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	$t_{RCD}$	25	65	ns
$t_{RLWL}$ Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	$t_{RWD}$	130		ns
$t_{WLCL}$ Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	$t_{WCS}$	-5		ns
$t_{rf}$ Refresh time interval	$t_{REF}$		4	ms

NOTE 1: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition,  $V_{IL}$  max and  $V_{IH}$  min must be met at the 10% and 90% points.

<sup>†</sup> All cycle times assume  $t_t = 5$  ns.

<sup>‡</sup> Page mode only.

<sup>§</sup> In a read-modify-write cycle,  $t_{CLWL}$  and  $t_{su}(WCH)$  must be observed. Depending on the user's transition times, this may require additional  $\overline{CAS}$  low time ( $t_w(CL)$ ). This applies to page-mode read-modify-write also.

<sup>¶</sup> In a read-modify-write cycle,  $t_{RLWL}$  and  $t_{su}(WRH)$  must be observed. Depending on the user's transition times, this may require additional  $\overline{RAS}$  low time ( $t_w(RL)$ ).

PARAMETER MEASUREMENT INFORMATION

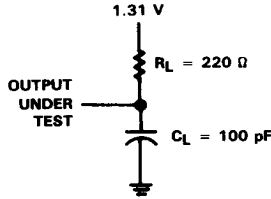
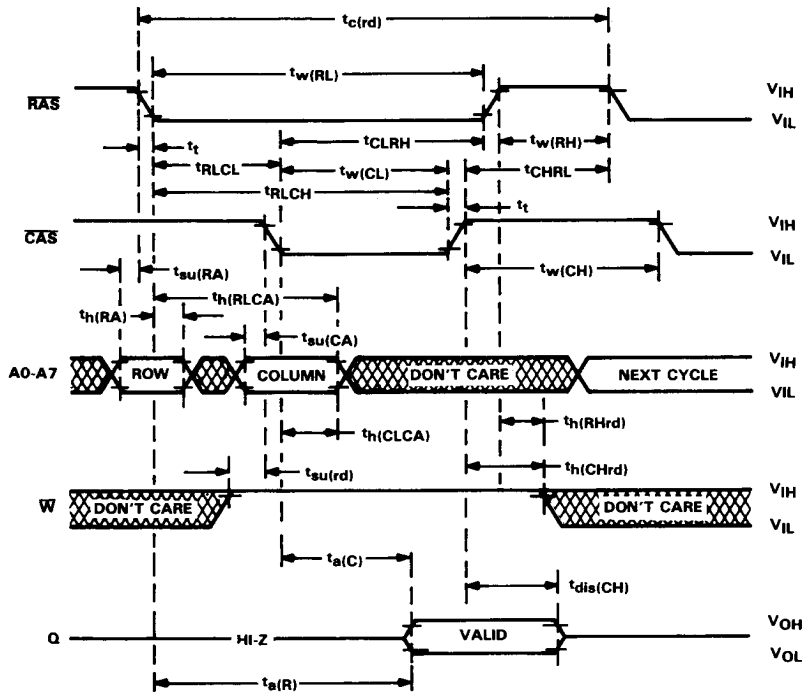


FIGURE 1. LOAD CIRCUIT

4

Dynamic RAMS

read cycle timing



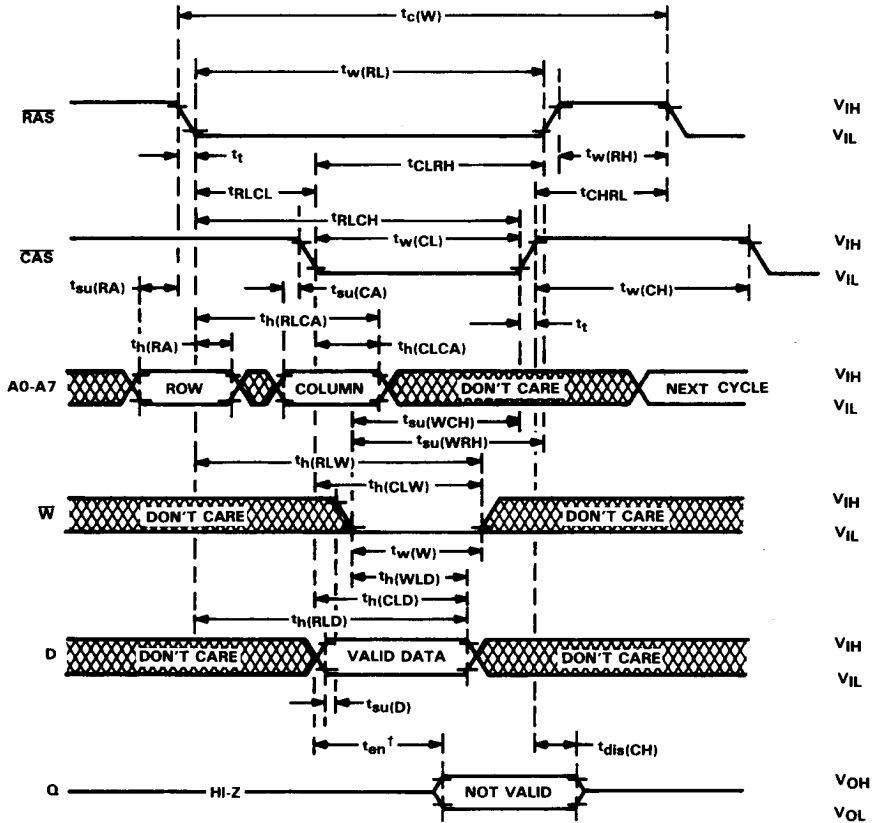


**TMS4164**  
**65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY**

**write cycle timing**

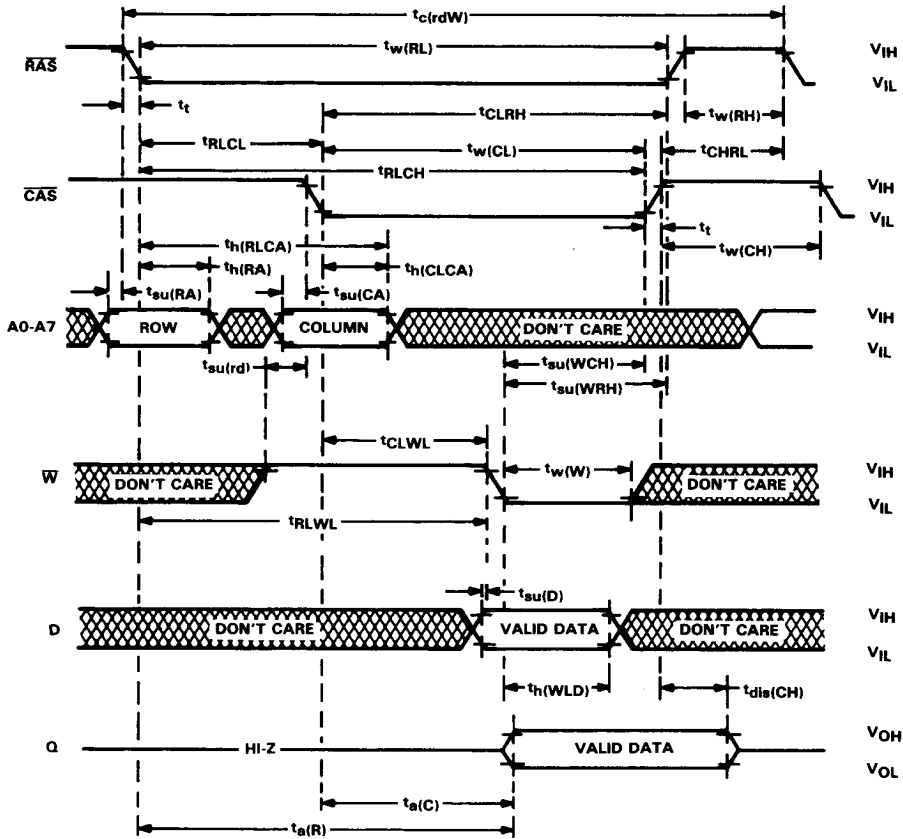
**4**

**Dynamic RAMs**



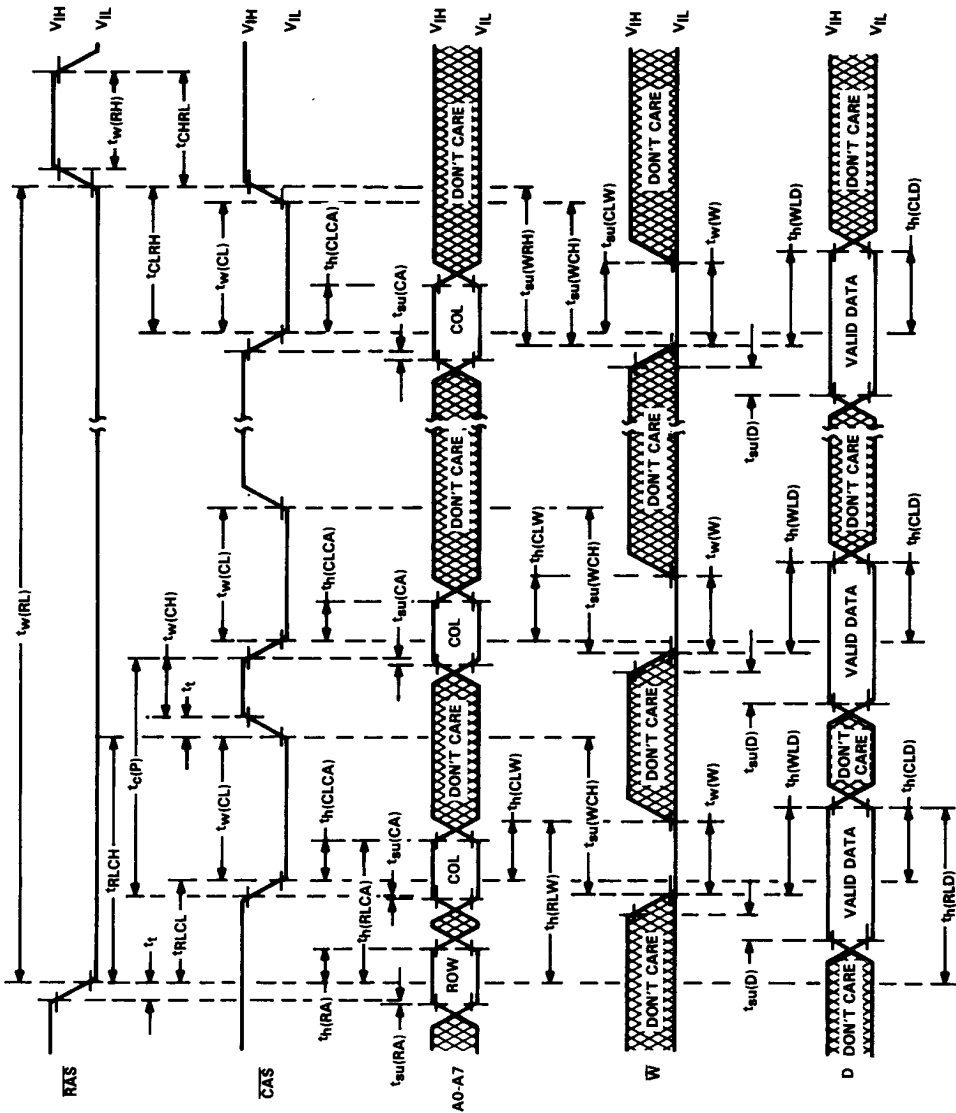
† The enable time ( $t_{en}$ ) for a write cycle is equal in duration to the access time from  $\overline{CAS}$  ( $t_{a}(C)$ ) in a read cycle; but the active levels at the output are invalid.

read-modify-write cycle timing





page-mode write cycle timing

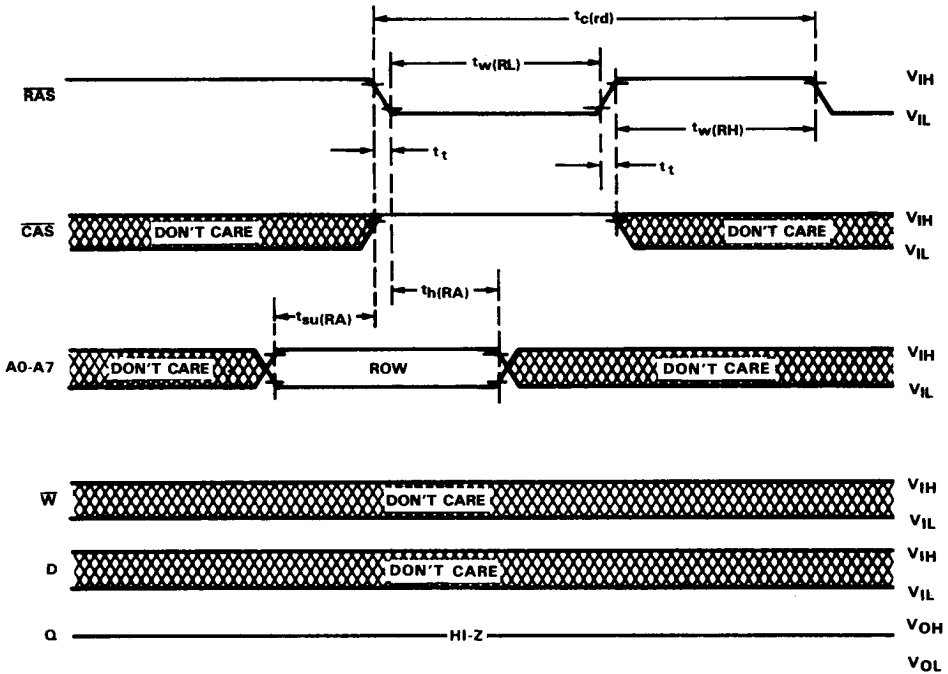


NOTE 3: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.



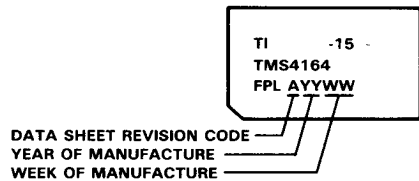
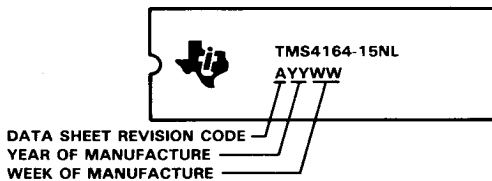


**RAS-only refresh timing**



**device symbolization**

This data sheet is applicable to all TI TMS4164 Dynamic RAMs with the code "A" to the left of the date code as shown below:

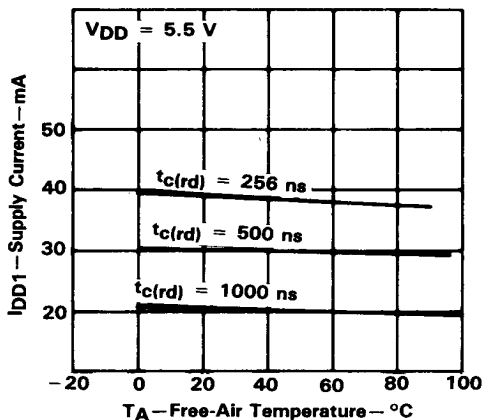


**TYPICAL CHARACTERISTICS**

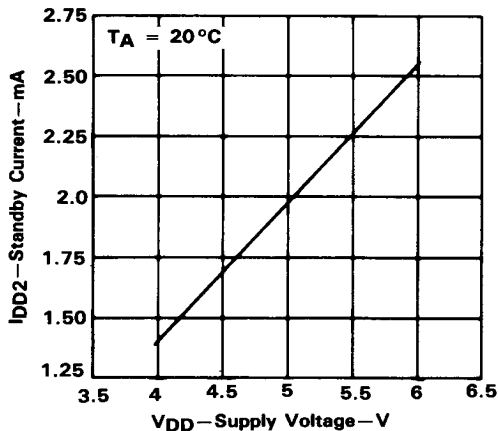
**4**

**Dynamic RAMs**

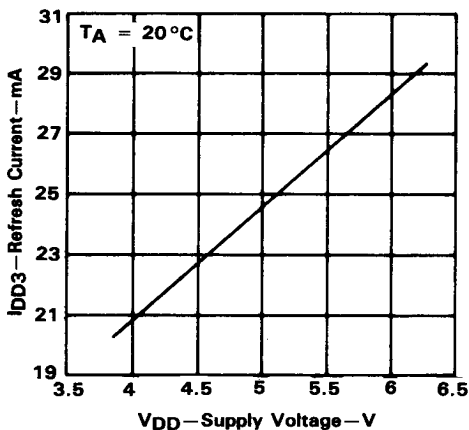
TYPICAL SUPPLY CURRENT  
 vs  
 FREE-AIR TEMPERATURE



TYPICAL SUPPLY CURRENT  
 vs  
 SUPPLY VOLTAGE



TYPICAL SUPPLY CURRENT  
 vs  
 SUPPLY VOLTAGE



TYPICAL SUPPLY CURRENT  
 vs  
 SUPPLY VOLTAGE

