Am26S02

Schottky Dual Retriggerable, Resettable Monostable Multivibrator

DISTINCTIVE CHARACTERISTICS

- Advanced Schottky technology with PNP inputs
- Retriggerable 0% to 100% duty cycle
- 28ns to ∞ output pulse width range
- 100kΩ maximum timing resistor value
- Am26S02XM typical pulse width change of only 1.0% over −55°C to +125°C with R_X = 100kΩ
- Am26S02XC typical pulse width change of only 0.4% over 0°C to +70°C with R_X = 100KΩ

GENERAL DESCRIPTION

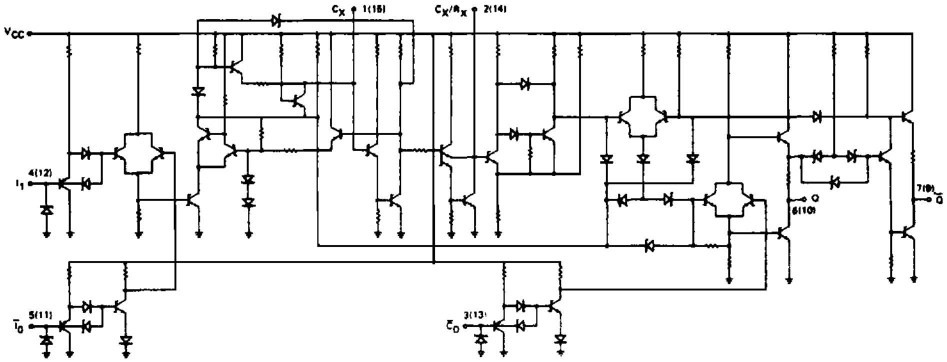
The Am26S02 is a dual DC level sensitive, retriggerable, resettable monostable multivibrator built using advanced Schottky technology. The output pulse duration and accuracy depend on the external timing components of each multivibrator. The Am26S02 features PNP inputs to reduce the input loading.

Provision is made on each multivibrator circuit for triggering the PNP inputs on either the rising or falling edge of an input signal by including an inverting and non-inverting trigger input. These PNP inputs are DC coupled making triggering independent of the input rise or fall time. Each time the monostable trigger input is activated from the OR trigger gate, full pulse length triggering occurs independent of the present state of the monostable.

The direct clear PNP input allows a timing cycle to be terminated at any time during the cycle. A LOW on the clear input forces the Q output LOW regardless of the $\bar{I}_0$ or I_1 inputs.

The Am26S02XM has a typical pulse width change of only 1.0% over the full military −55°C to +125°C temperature range and the Am26S02XC has a typical pulse width change of only 0.4% over the commerical 0°C to +70°C temperature range with a R_X = 100kΩ.

SCHEMATIC DIAGRAM
(One Monostable Multivibrator Shown)



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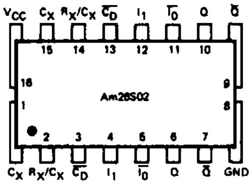
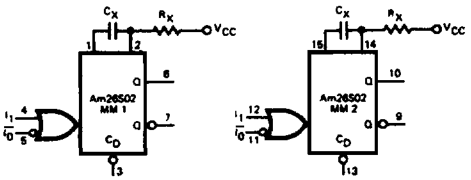
CONNECTION DIAGRAM
Top View



CD003050

Note: Pin 1 is marked for orientation

LOGIC SYMBOL



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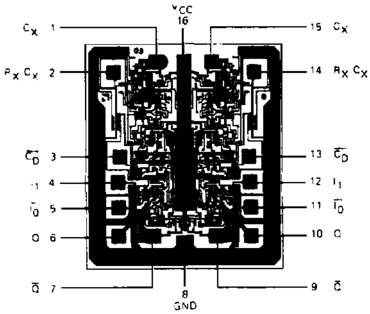
V_{CC} = Pin 16
GND = Pin 8

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.062" x 0.071"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am26S02 D C B

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 16-pin CERDIP
  - F – 16-pin flatpak
  - P – 16-pin plastic DIP
  - X – Dice
- **Am26S02** — Device type
  - Schottky Dual Multivibrator

Valid Combinations	
Am26S02	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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PIN DESCRIPTION

Pin No.	Name	I/O	Description
13	$\bar{C}_D$	I	Asynchronous direct CLEAR. A LOW on the clear input resets the monostable regardless of the other inputs.
11	$\bar{I}_0$	I	Active-LOW input. With I_1 LOW, a HIGH-to-LOW transition will trigger the monostable.
12	I_1	I	Active-HIGH input. With $\bar{I}_0$ HIGH, a LOW-to-HIGH transition will trigger the monostable.
10	Q	O	The TRUE monostable output.
9	$\bar{Q}$	O	The Complement monostable output.

FUNCTION TABLE

INPUTS			OUTPUTS	
OSC_D	I_1	I_1	$\bar{I}_0$	Q
L	X	X	L	H
H	H	X	L	H
H	L	↓	⎍	⊔
H	X	L	L	H
H	↑	H	⎍	⊔

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition
↓ = HIGH-to-LOW Transition
⎍ = LOW-HIGH-LOW Pulse
⊔ = HIGH-LOW-HIGH Pulse
X = Don't Care

LOADING RULES (In Unit Loads)

Input/ Output		Pins No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
C_X	Mono 1	1	–	–	–
R_X/C_X		2	–	–	–
$\bar{C}_D$		3	0.4	–	–
I_1		4	0.4	–	–
$\bar{I}_0$		5	0.4	–	–
Q		6	–	40	10
$\bar{Q}$		7	–	40	10
GND		8	–	–	–
$\bar{Q}$	Mono 2	9	–	40	10
Q		10	–	40	10
$\bar{I}_0$		11	0.4	–	–
I_1		12	0.4	–	–
$\bar{C}_D$		13	0.4	–	–
R_X/C_X		14	–	–	–
C_X		15	–	–	–
V_{CC}		16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

OPERATION RULES

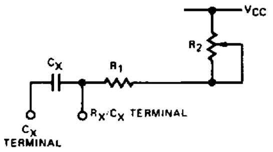
TIMING

1. Timing components C_x and R_x values.

Operating Temperature Range

	0°C to 70°C	−55°C to +125°C
R_X MIN	5kΩ	5kΩ
R_X MAX	100kΩ	50kΩ
C_X	any value	any value

2. Remote adjustment of timing.



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$$R_1 + R_2 = R_x$$
$$R_1 \geq R_x MIN.$$
$$R_2 < R_x MAX. - R_1$$

In the above arrangement, R_1 and C_x should be as close as possible to the device pins to minimize stray capacitance and external noise pickup. The variable resistor R_2 can be located remotely from the device if reasonable care is used.

Refer to Page 13-1 for Essential Information on Military Devices

OPERATION RULES (Cont.)

3. Pulse width change measurements.

The pulse width $t_{pw}Q$ is specified and measured with components of better than 0.1% accuracy. If measurements are made with reduced component tolerances, the expected accuracy should be adjusted accordingly. Note that pulse width temperature stability improves as R_X increases.

4. Timing for $C_X \leq 1000$ pF.

When using capacitor of less than or equal to 1000 pF in value, the output pulse width should be determined from the output pulse width versus external timing capacitance graph.

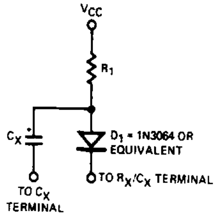
5. Timing for $C_X > 1000$ pF.

For capacitors of greater than 1000 pF in value, the output pulse width, $t_{pw}Q$, is determined by:

$$t_{pw}Q = 0.30 C_X R_X \left(1 + \frac{0.11}{R_X}\right)$$

where

R_X is in kilohms
C_X is in picofarads
$t_{pw}Q$ is in nanoseconds



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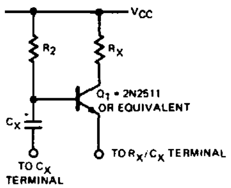
$R_1 \leq 0.6 \times R_X$ MAX.



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$R_2 < 0.7 \times h_{FEQ1} \times R_X$

6. Protection of electrolytic timing capacitors.

If the electrolytic capacitor to be used as C_X cannot withstand 1.0 volt reverse bias, one of the two circuit techniques shown below should be used to protect the electrolytic capacitor from the reverse voltage. The accuracy of the pulse width may be dependent on the diode (transistor) characteristics.

The output pulse width, $t_{pw}Q$ for the diode circuit modifies the previous timing equation as follows:

$$t_{pw}Q = 0.26 C_X R_X \left(1 + \frac{0.13}{R_X}\right)$$

The output pulse width for the transistor circuit is:

$$t_{pw}Q = 0.21 C_X R_X \left(1 + \frac{0.16}{R_X}\right)$$

Notice that the transistor circuit allows values of timing resistor R_2 larger than the R_X MIN. $< R_X < R_X$MAX. to obtain longer output pulse widths for a given C_X.

TRIGGER AND RETRIGGER

1. Triggering.

The minimum pulse width signal into input $\bar{I}_0$ or input I_1 to cause the device to trigger is 20ns. Refer to the truth table for the appropriate input conditions.

2. Retriggering.

The retriggered pulse width, $t_{pwr}Q$, is the time during which the output is active after the device is retriggered during a timing cycle. *It differs from the initial pulse width $t_{pw}Q$ timing* equations as follows:

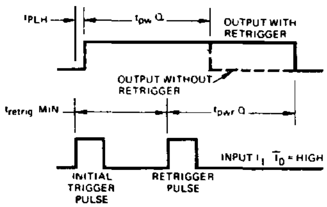
$$t_{pwr}Q = t_{pw}Q + t_{PLH}$$

where t_{PLH} is the propagation delay time from the $\bar{I}_0$ or I_1 input to the output. Note that t_{PLH} is typically 14ns and therefore becomes relatively unimportant as $t_{pw}Q$ increases.

3. Rapid retriggering.

A minimum retriggering time does exist. That is, the device cannot be retriggered until a minimum recovery time has elapsed. The minimum retrigger time is approximately:

t_{retrig}MIN. $= 0.2C_X$
C is in picofarads
t is in nanoseconds



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CLEAR

A LOW on the clear inputs terminates the timing cycle. A new trigger cycle cannot be initiated while the clear is LOW. With the clear HIGH, the device is under the command of the I_1 and $\bar{I}_0$ inputs.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65°C to +150°C
Ambient Temperature Under Bias .... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 16 to Pin 8) Continuous .... −0.5V to +7.0V
DC Voltage Applied to Outputs For
HIGH Output State .... −0.5V to $+V_{CC}$ max
DC Input Voltage .... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current .... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature .... 0°C to +70°C
Supply Voltage .... +4.75V to +5.25V

Military (M) Devices
Temperature .... −55°C to +125°C
Supply Voltage .... +4.5V to +5.5V

Operating ranges define limits over which the functionality of the device is guaranteed.

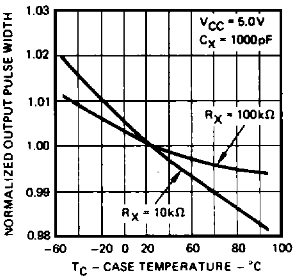
DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)	Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2mA V_{IN} = V_{IH} or V_{IL}	2.5	2.8		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}		0.38	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA		−0.4	−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V		−0.15	−0.4	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		0.1	20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V			1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX, V_{OUT} = 1.0V T_A = 25°C Only	−8	−15	−35	mA
I_{CC}	Power Supply Current	V_{CC} = 5.0V, I_{IX} = 0.33mA (Notes 5 & 6)		48	69	mA

Notes:
1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN. or MAX. use the appropriate value specified under Electrical Characteristics for the applicable device type.
3. Actual input currents = Unit Load x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with pin 5 and 11 grounded and I_{IX} applied to pins 2 and 14.
6. I_{IX} is the current into the R_XC_X node to simulate R_X.

TYPICAL PERFORMANCE CURVES

Typical Normalized Output Pulse Width Versus Case Temperature



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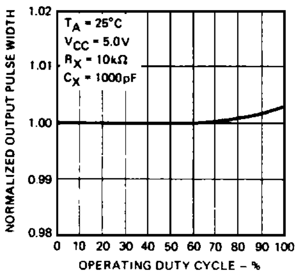
Normalized Output Pulse Width Versus Operating Duty Cycle



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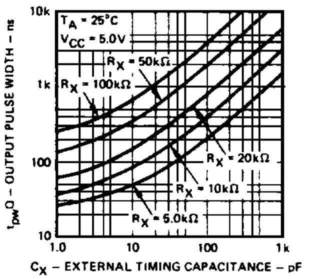
Output Pulse Width Versus External Timing Capacitance



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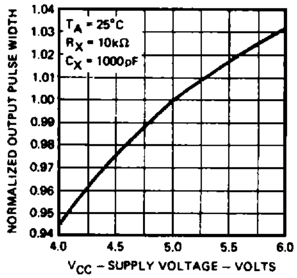
Typical Normalized Output Pulse Width Versus Supply Voltage



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SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PLH}	$\bar{I}_0$ to Q		V_{CC} = 5.0 V, R_L = 280 Ω, C_L = 15 pF, R_X = 5 kΩ, C_X = 0 pF		13	20	ns
t_{PHL}	$\bar{I}_0$ to $\bar{Q}$				15	23	ns
t_{PLH}	I_1 to Q				12	20	ns
t_{PHL}	I_1 to $\bar{Q}$				12	20	ns
t_{PLH}	Clear to $\bar{Q}$				21		ns
t_{PHL}	Clear to Q				9	13	ns
t_{pw}	Pulse Width	$\bar{I}_0$ HIGH or I_1 LOW		20	10		ns
		$\bar{I}_0$ LOW to I_1 HIGH		16	7		ns
		Clear LOW		24	16		ns
t_s	Clear Recovery (inactive) to Trigger			−10	−22		ns
t_{pw}Q (Min)	Minimum Pulse Width Q Output		V_{CC} = 5.0 V, R_X = 5.0 kΩ, C_X = 0 pF, R_L = 1.0 kΩ	27	33	39	ns
t_{pw}Q	Pulse Width Q Output		V_{CC} = 5.0 V, R_L = 280 Ω, C_L = 15 pF, R_X = 10 kΩ, C_X = 1000 pF (CK05 Type)	3.23	3.42	3.61	μs
R_X	Timing Resistor		0°C to 70°C	5		100	kΩ
			−55°C to +125°C	5		50	

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