

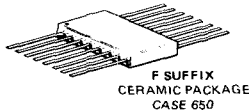
MC1600 Series (-30°C to +85°C)

The requirement for digital systems with ever higher performance has increased the need for high-speed integrated circuits. The industry has recognized that the only economical way to obtain high operating system speed is through the use of emitter-coupled logic. Motorola offers a state-of-the-art, emitter-coupled logic family with subnanosecond propagation delays — MECL III.

MECL III circuit design is similar to that used in the popular MECL 10,000 family. In the MECL III line, as well as MECL 10,000, advanced processing techniques are employed and the capability for driving low-impedance terminated lines is provided. MECL III is recommended for new designs.

### GENERAL FEATURES

- Gate Switching Speeds of 1.0 ns typical
- Capability of Driving Terminated Lines with Impedance as Low as 50 Ohms
- Flip-Flop Toggle Rate Greater Than 500 MHz
- Operation with Unused Inputs Left Open
- Multilayer Metalization for economy
- New Packages with Improved Electrical and Thermal Characteristics
- Compatibility with MECL 10,000 Series
- Counting Speeds to above 1 GHz



### FUNCTIONS AND CHARACTERISTICS (V<sub>CC</sub> = 0, V<sub>EE</sub> = -5.2 V, T<sub>A</sub> = 25°C unless otherwise noted.)

Function	Type ① -30° to +85°C	Loading Factor # Each Output	Propagation Delay 50-ohm Load ns typ	Power Dissipation (No Load) mW typ/pkg	Case
Voltage Controlled Oscillator	MC1648	—	*225 MHz typ	150	607,632,646
Dual A/D Comparator	MC1650	70	3.5	275	620,650
Dual A/D Comparator	MC1651	70	3.0	275	620,650
Binary Counter	MC1654	70	*325 MHz typ	750 <i>LLL</i>	620
Voltage-Controlled Multivibrator	MC1658	70	*150 MHz typ	125	620,648,650
Dual 4-Input OR/NOR Gate	MC1660	70	1.1	120	620,650
Quad 2-Input NOR Gate	MC1662	70	1.1	240	620,650
Quad 2-Input OR Gate	MC1664	70	1.1	240	620,650
Dual Clocked R-S Flip-Flop	MC1666	70	1.8	220	620,650
Dual Clocked Latch	MC1668	70	1.8	220	620,650
Master-Slave Type D Flip-Flop	MC1670	70	*350 MHz typ	220	620,650
Triple 2-Input Exclusive OR Gate	MC1672	70	1.3	220	620,650
Triple 2-Input Exclusive NOR Gate	MC1674	70	1.3	220	620,650
Bi-Quinary Counter	MC1678	70	*350 MHz typ	750 <i>LLL</i>	620
Dual 4-5-Input OR/NOR Gate	MC1688	70	0.8	125	650
UHF Prescaler Type D Flip-Flop	MC1690	70	*500 MHz min	200	620,650
Quad Line Receiver	MC1692	70	1.1	220	620,650
4-Bit Shift Register	MC1694	70	*325 MHz typ	750 <i>LLL</i>	620
1 GHz Divide-By-Ten Counter	MC1696	—	*1 GHz min	650	650

① L suffix denotes Dual In-Line Ceramic Package, F suffix denotes Ceramic Flat Package, P suffix denotes Dual In-Line Plastic Package. (i.e., MC1600L = Ceramic Dual In-Line Package, MC1600F = Ceramic Flat Package, MC1600P = Plastic Dual In-Line Package).

*LLL* Requires Heat Sink — IERC-LIC-214A2WCB or equivalent.

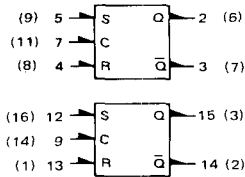
\*Toggle Frequency

#DC Loading Factors are based on:

1. Full load output current, I<sub>L</sub> = -25 mA<sub>dc</sub> max
2. Maximum input current, I<sub>in</sub> = 350 μA<sub>dc</sub>

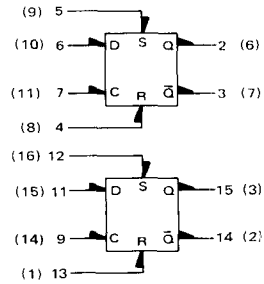
FLIP-FLOPS

**MC1666**  
Dual Clocked R-S Flip-Flop



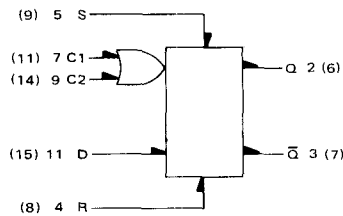
$t_{pd} = 1.6 \text{ ns typ (510-ohm load)}$   
 $= 1.8 \text{ ns typ (50-ohm load)}$   
 $P_D = 220 \text{ mW typ/pkg (no-load)}$

**MC1668**  
Dual Clocked Latch



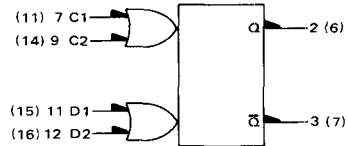
$t_{pd} = 1.6 \text{ ns typ (510-ohm load)}$   
 $= 1.8 \text{ ns typ (50-ohm load)}$   
 $P_D = 220 \text{ mW typ/pkg (no-load)}$

**MC1670**  
Master-Slave Type D Flip-Flop



$f_{Tog} = 350 \text{ MHz typ}$   
 $P_D = 220 \text{ mW typ/pkg (no load)}$

**MC1690**  
UHF Prescaler Type D Flip-Flop

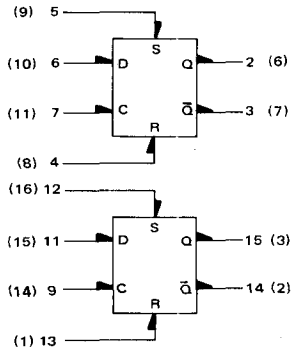


$f_{Tog} = 500 \text{ MHz min}$   
 $P_D = 200 \text{ mW typ/pkg (No Load)}$

MC1668

This device is a Dual Clocked Latch/R-S Flip-Flop. Whenever the Clock is low, the R-S inputs control the output state. Whenever the Clock is high, the output follows the data (D) input.

POSITIVE LOGIC



S	R	D	C	Q <sub>n+1</sub>
0	0	φ	0	Q <sub>n</sub>
1	0	φ	0	1
0	1	φ	0	0
1	1	φ	0	**
φ	φ	0	1	0
φ	φ	1	1	1

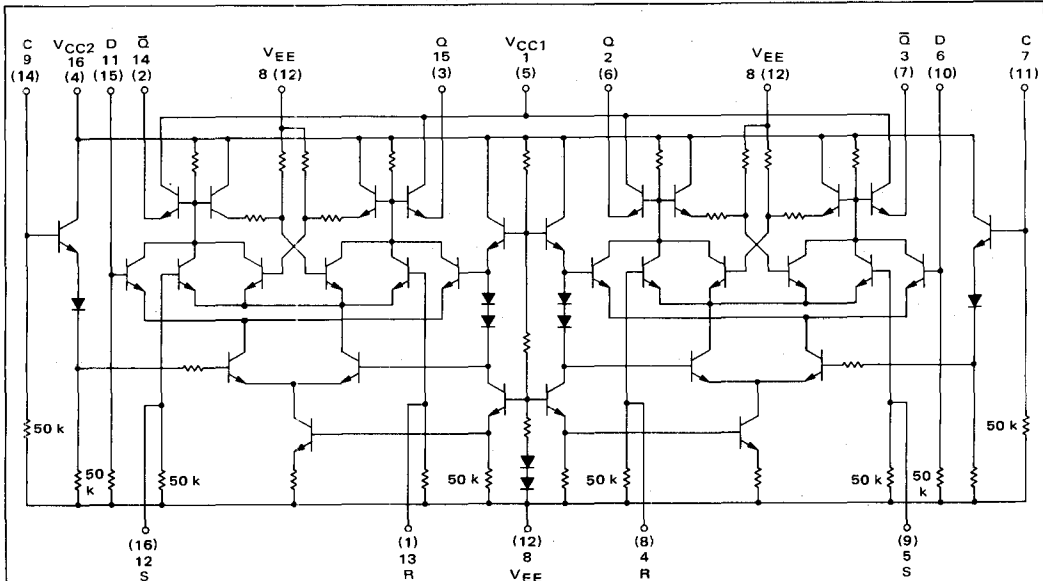
\*\*Output state not defined φ = Don't Care

VCC1 = Pin 1 (5)  
 VCC2 = Pin 16 (4)  
 VEE = Pin 8 (12)

t<sub>pd</sub> = 1.6 ns typ (510-ohm load)  
 = 1.8 ns typ (50-ohm load)  
 P<sub>D</sub> = 220 mW typ/pkg (No load)

Numbers at ends of terminals denote pin numbers for L package (Case 620).  
 Numbers in parenthesis denote pin numbers for F package (Case 650).

CIRCUIT SCHEMATIC



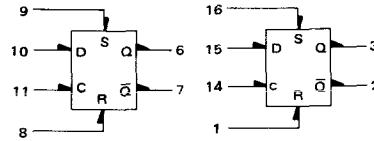
Numbers at ends of terminals denote pin numbers for L package (Case 620).  
 Numbers in parenthesis denote pin numbers for F package (Case 650).

See General Information section for packaging.



### ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. Air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



**F SUFFIX**  
**CERAMIC PACKAGE**  
**CASE 650**



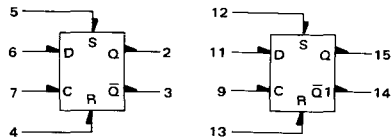
@Test Temperature	TEST VOLTAGE VALUES (Volts)				
	V <sub>IH</sub> max	V <sub>IL</sub> min	V <sub>IHA</sub> min	V <sub>I LA</sub> max	V <sub>EE</sub>
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC1668F Test Limits						Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					(V <sub>CC</sub> ) Gnd
			-30°C		+25°C		+85°C			V <sub>IH</sub> max	V <sub>IL</sub> min	V <sub>IHA</sub> min	V <sub>I LA</sub> max	V <sub>EE</sub>	
			Min	Max	Min	Max	Min	Max							
Power Supply Drain Current	I <sub>E</sub>	12 ①	-	-	-	55	-	-	mAdc	11, 14	-	-	-	12	4.5
Input Current	I <sub>in</sub> H	1, 15, 16 ②	-	-	-	0.370	-	-	mAdc	1, 15, 16	-	-	-	12	4.5
		13	-	-	-	0.225	-	-	mAdc	14	-	-	-	12	4.5
I <sub>in</sub> L	I <sub>in</sub> L	1, 15, 16 ②	-	-	0.500	-	-	-	μAdc	-	1, 15, 16	-	-	12	4.5
		13	-	-	0.500	-	-	-	μAdc	-	14	-	-	12	4.5
"Q" Logic "1" Output Voltage	V <sub>OH</sub>	3 ③ 3 ④	-1.045	-0.875	-0.960	-1.810	-0.890	-0.700	Vdc	-	1	-	-	12	4.5
"Q" Logic "0" Output Voltage	V <sub>OL</sub>	3 ⑤	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	-	16	-	-	12	4.5
		3 ⑥	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	14	-	-	-	12	4.5
"Q" Logic "1" Output Voltage	V <sub>OH</sub>	2 ⑤	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	-	16	-	-	12	4.5
		2 ⑥	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	14	-	-	-	12	4.5
"Q" Logic "0" Output Voltage	V <sub>OL</sub>	2 ④	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	-	1	-	-	12	4.5
		2 ④	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	14	-	-	-	12	4.5
"Q" Logic "1" Output Threshold Voltage	V <sub>OHA</sub>	3	-1.065	-	-0.980	-	-0.910	-	Vdc	-	-	16	1	12	4.5
		3 ⑦ 3 ⑧	↓	-	↓	-	↓	-	↓	15	-	15	-	↓	↓
"Q" Logic "0" Output Threshold Voltage	V <sub>OLA</sub>	3	-	-1.630	-	-1.600	-	-1.555	Vdc	-	-	1	16	12	4.5
		3 ⑥ 3 ⑨	-	↓	-	↓	-	↓	-	-	15	14	-	↓	↓
"Q" Logic "1" Output Threshold Voltage	V <sub>OHA</sub>	2	-1.065	-	-0.980	-	-0.910	-	Vdc	-	-	1	16	12	4.5
		2 ⑥ 2 ⑩	↓	-	↓	-	↓	-	↓	-	15	14	-	↓	↓
"Q" Logic "0" Output Threshold Voltage	V <sub>OLA</sub>	2	-	-1.630	-	-1.600	-	-1.555	Vdc	-	-	16	1	12	4.5
		2 ⑦ 2 ⑪	-	↓	-	↓	-	↓	-	-	15	-	-	↓	↓
Switching Times (50 Ω Load) Clock Input	t <sub>13+3+</sub> t <sub>13+3-</sub> t <sub>13+2-</sub> t <sub>13+2+</sub>	3	1.0	2.7	1.0	2.5	1.1	2.8	ns	Pulse In 14	Pulse Out 3	-	-	-3.2 V	+2.0 V
		3	↓	↓	↓	↓	↓	↓	↓	↓	3	-	-	↓	↓
		2	↓	↓	↓	↓	↓	↓	↓	↓	2	-	-	↓	↓
		2	↓	↓	↓	↓	↓	↓	↓	↓	2	-	-	↓	↓
Rise Time	t <sub>r</sub>	2, 3	0.8	2.8	0.9	2.5	0.9	2.9	ns	14	2, 3	-	-	12	4.5
Fall Time	t <sub>f</sub>	2, 3	0.5	2.4	0.5	2.2	0.5	2.6	ns	14	2, 3	-	-	12	4.5
Set Input	t <sub>16+3+</sub> t <sub>16+2-</sub>	3	1.0	2.5	1.1	2.3	1.1	2.7	ns	16	3	-	-	12	4.5
		2	1.0	2.5	1.1	2.3	1.1	2.7	ns	16	2	-	-	12	4.5
Reset Input	t <sub>1+2+</sub> t <sub>1+3-</sub>	2	1.0	2.5	1.1	2.3	1.1	2.7	ns	1	2	-	-	12	4.5
		3	1.0	2.5	1.1	2.3	1.1	2.7	ns	1	3	-	-	12	4.5

①Notes appear on page following Electrical Characteristics tables.

**ELECTRICAL CHARACTERISTICS**

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



**L SUFFIX  
CERAMIC PACKAGE  
CASE 620**

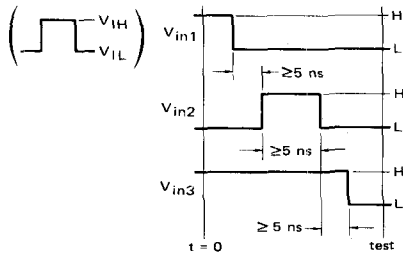
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Characteristic	Symbol	Pin Under Test	MC1668L Test Limits						Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					(V <sub>CC</sub> ) Gnd
			-30°C		+25°C		+85°C			V <sub>IH</sub> max	V <sub>IL</sub> min	V <sub>IHA</sub> min	V <sub>ILA</sub> max	V <sub>EE</sub>	
			Min	Max	Min	Max	Min	Max							
Power Supply Drain Current	I <sub>E</sub> (H-Z) I	8	-	-	-	55	-	-	mAdc	7,9	-	-	-	8	1,16
Input Current	I <sub>in</sub> H	11,12,13 ②	-	-	-	0.370	-	-	mAdc	11,12,13	-	-	-	8	1,16
		9	-	-	-	0.225	-	-	mAdc	9	-	-	-	8	1,16
Input Current	I <sub>in</sub> L	11,12,13 ②	-	-	0.500	-	-	-	μAdc	-	11,12,13	-	-	8	1,16
		9	-	-	0.500	-	-	-	μAdc	-	9	-	-	8	1,16
"Q" Logic "1" Output Voltage	V <sub>OH</sub>	15 ③ 15 ④	-1.045 -1.045	-0.875 -0.875	-0.960 -0.960	-1.810 -1.810	-0.890 -0.890	-0.700 -0.700	Vdc	9	13	-	-	8	1,16
"Q" Logic "0" Output Voltage	V <sub>OL</sub>	15 ⑤	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	-	12	-	-	8	1,16
		15 ⑥	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	-	-	-	8	1,16
"Q-bar" Logic "1" Output Voltage	V <sub>OH</sub>	14 ⑤	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	-	12	-	-	8	1,16
		14 ⑥	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	9	-	-	-	8	1,16
"Q-bar" Logic "0" Output Voltage	V <sub>OL</sub>	14 ③	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	-	13	-	-	8	1,16
		14 ④	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	-	-	-	8	1,16
"Q" Logic "1" Output Threshold Voltage	V <sub>OHA</sub>	15 ⑦	-1.065	-	-0.980	-	-0.910	-	Vdc	-	-	12	13	8	1,16
		15 ⑤	-	-	-	-	-	-	Vdc	11	-	11	-	8	1,16
"Q" Logic "0" Output Threshold Voltage	V <sub>OLA</sub>	15 ⑥	-	-1.630	-	-1.600	-	-1.555	Vdc	-	-	13	12	8	1,16
		15 ③	-	-	-	-	-	-	Vdc	-	-	11	11	8	1,16
		15 ④	-	-	-	-	-	-	Vdc	-	-	11	9	8	1,16
"Q-bar" Logic "1" Output Threshold Voltage	V <sub>OLA</sub>	14 ⑥	-1.065	-	-0.980	-	-0.910	-	Vdc	-	-	13	12	8	1,16
		14 ③	-	-	-	-	-	-	Vdc	-	-	11	11	8	1,16
		14 ④	-	-	-	-	-	-	Vdc	-	-	11	9	8	1,16
"Q-bar" Logic "0" Output Threshold Voltage	V <sub>OLA</sub>	14 ⑦	-	-1.630	-	-1.600	-	-1.555	Vdc	-	-	12	13	8	1,16
		14 ⑤	-	-	-	-	-	-	Vdc	-	-	11	11	8	1,16
		14 ⑥	-	-	-	-	-	-	Vdc	-	-	9	9	8	1,16
Switching Times (50 Ω Load) Clock Input	t <sub>9+15+</sub> t <sub>9+15-</sub> t <sub>9+14+</sub> t <sub>9+14-</sub>	15	1.0	2.7	1.0	2.5	1.1	2.8	ns	9	15	-	-	8	1,16
		15	↓	↓	↓	↓	↓	↓	ns	↓	15	-	-	8	1,16
		14	↓	↓	↓	↓	↓	↓	ns	↓	14	-	-	8	1,16
		14	↓	↓	↓	↓	↓	↓	ns	↓	14	-	-	8	1,16
Rise Time	t <sub>r</sub>	14,15	0.8	2.8	0.9	2.5	0.9	2.9	ns	9	14,15	-	-	8	1,16
Fall Time	t <sub>f</sub>	14,15	0.5	2.4	0.5	2.2	0.5	2.6	ns	9	14,15	-	-	8	1,16
Set Input	t <sub>12+15+</sub> t <sub>12+14-</sub>	15	1.0	2.5	1.1	2.3	1.1	2.7	ns	12	15	-	-	8	1,16
		14	1.0	2.5	1.1	2.3	1.1	2.7	ns	12	14	-	-	8	1,16
Reset Input	t <sub>13+14+</sub> t <sub>13+15-</sub>	14	1.0	2.5	1.1	2.3	1.1	2.7	ns	13	14	-	-	8	1,16
		15	1.0	2.5	1.1	2.3	1.1	2.7	ns	13	15	-	-	8	1,16

① Notes appear on page following Electrical Characteristics tables.

NOTES

- ①  $I_E$  is measured with no output pulldown resistors.
- ② Test voltage applied to pin under test.



- ③ Apply  $V_{in1}$  to S ( $V_{IH}$  to  $V_{IL}$ ).
- ④ Apply Sequentially:  $V_{in1}$  to R ( $V_{IH}$  to  $V_{IL}$ )  
 $V_{in2}$  to C ( $V_{IH}$ ,  $V_{IL}$ )  
 $V_{in3}$  to D ( $V_{IH}$  to  $V_{IL}$ )
- ⑤ Apply  $V_{in1}$  to R ( $V_{IH}$  to  $V_{IL}$ )
- ⑥ Apply Sequentially:  $V_{in1}$  to S ( $V_{IH}$  to  $V_{IL}$ )  
 $V_{in2}$  to C ( $V_{IH}$ ,  $V_{IL}$ )
- ⑦ Apply Sequentially:  $V_{in1}$  to R ( $V_{IH}$  to  $V_{IL}$ )  
 $V_{in2}$  to C ( $V_{IH}$ ,  $V_{IL}$ )

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS @ 25°C

