SGS-THOMSON MICROELECTRONICS

MK6264(N,S)70/120
MK6264L(N,S)70/120
MK6264U(N,S)70/120

64K (8K x 8-BIT) CMOS STATIC RAM

FEATURES

- 70 And 120 ns Address Access Time
- Equal Access And Cycle Times
- Static Operation - No Clocks Or Timing Strobes Required
- Low Vcc Data Retention 2 Volts
- All Inputs And Outputs Are CMOS And TTL Compatible
- Full CMOS 6-T Cell
- Three State Output
- Standard 28-Pin Package In 600 Mil Plastic DIP Or 330 Mil SOIC Package

PIN NAMES

A0 - A12	Address Inputs
DQ0 - DQ7	Data Input/Output
$\overline{E1}$, E2	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
Vcc	+5V
Vss	Ground
N/C	No Connection

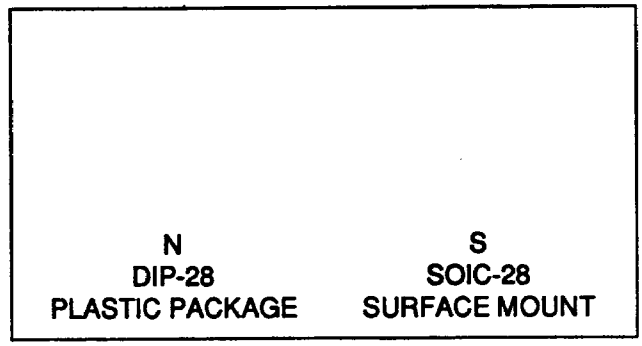
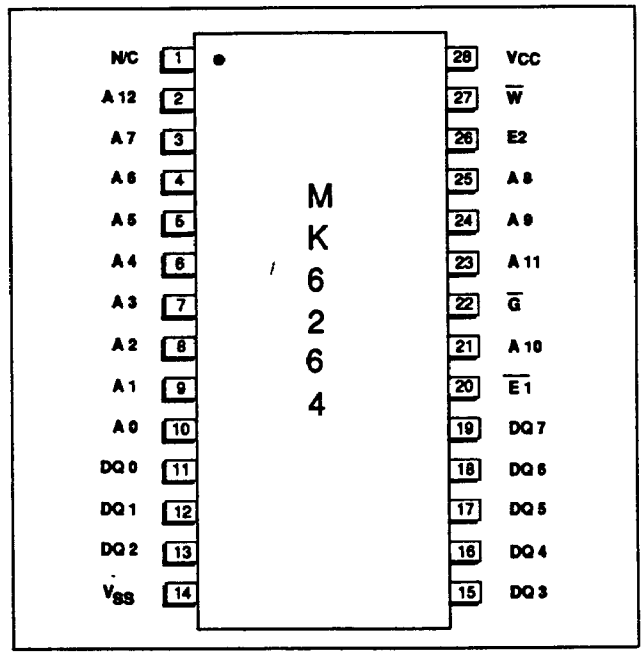


Figure 1. PIN CONNECTIONS



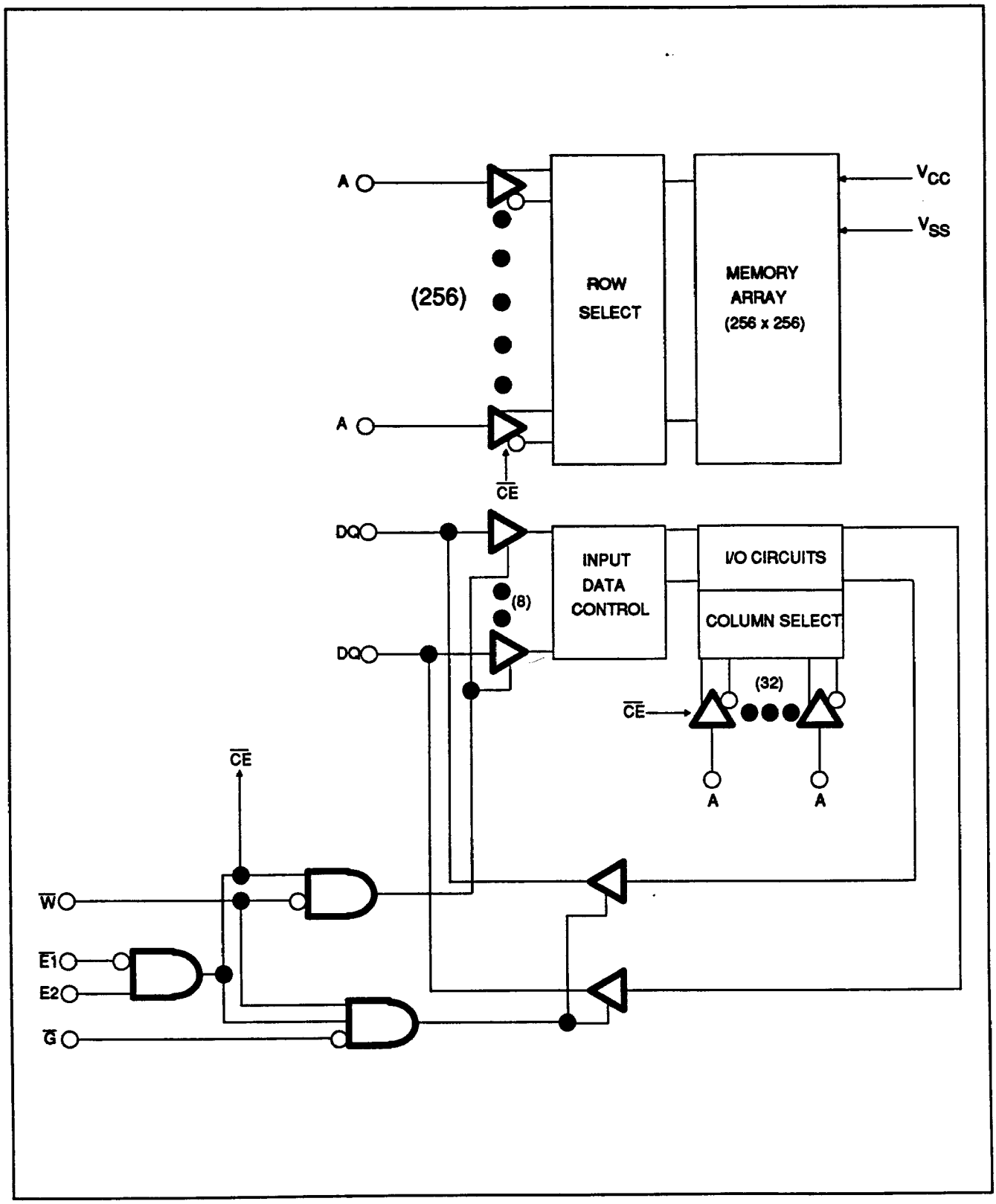
DESCRIPTION

The MK6264 is a 65,536-bit static RAM, organized as 8K X 8 bits. It is fabricated using SGS-Thomson's low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single +5V ± 10% supply, and is fully TTL compatible.

The MK6264 has a Chip Enable power down feature which sustains an automatic standby mode whenever either Chip Enable goes inactive ($\overline{E1}$ goes high or E2 goes low). An Output Enable ($\overline{G}$) pin provides a high speed tristate control, allowing fast read/write cycles to be achieved with the common-I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{G}$, $\overline{E1}$ and E2, as summarized in the truth table.

The MK6264 is available in a 600 Mil Plastic DIP, or a 330 Mil SOIC package.

Figure 2. FUNCTIONAL BLOCK DIAGRAM



MK6264 TRUTH TABLE

$\overline{W}$	$\overline{E1}$	E2	$\overline{G}$	MODE	DQ	POWER
X	H	X	X	Deselect	High-Z	Standby
X	X	L	X	Deselect	High-Z	Standby
H	L	H	H	Read	High-Z	Active
H	L	H	L	Read	Q_{OUT}	Active
L	L	H	X	Write	D_{IN}	Active

OPERATIONS

READ MODE

The MK6264 is in the Read mode whenever Write Enable ($\overline{W}$) is high with Output Enable ($\overline{G}$) low, and both Chip Enables (E1 and E2) are active. This provides access to data from eight of 65,536 locations in the static memory array. The unique address specified by 13 Address Inputs defines which one of the 8192x8-bit bytes is to be accessed. Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is low, $\overline{E1}$ is low, and E2 is high. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV}, t_{E2HQV}, or t_{GLQV}) rather than the address. The state of the DQ pins is controlled by the $\overline{E1}$, E2, $\overline{G}$, and $\overline{W}$ control signals. Data out may be indeterminate at t_{E1LQX}, t_{E2HQX}, and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

READ CYCLE TIMING

{0° C ≤ T_A ≤ 70° C , Vcc = 5.0 V ± 10 %}

SYMBOLS		PARAMETERS	MK6264-70 MK6264L-70 MK6264U-70		MK6264-120 MK6264L-120 MK6264U-120			
ALT.	STD.		MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	t_{AVAV}	Read Cycle Time	70		120		ns	
t_{AA}	t_{AVQV}	Address Access Time		70		120	ns	1
t_{CEA} 1 & 2	t_{E1LQV} t_{E2HQV}	Chip Enable 1 & 2 Access Time		70 70		120 120	ns ns	1
t_{OEA}	t_{GLQV}	Output Enable AccessTime		35		50	ns	1
t_{CEL} 1 & 2	t_{E1LQX} t_{E2HQX}	Chip Enable 1 & 2 to Output Low-Z	5 5		5 5		ns ns	2
t_{OEL}	t_{GLQX}	Output Enable to Low-Z	0		0		ns	2
t_{CEZ} 1& 2	t_{E1HQZ} t_{E2LQZ}	Chip Enable 1 & 2 to High-Z		30 30		40 40	ns ns	2
t_{OEZ}	t_{GHQZ}	Output Enable to High-Z		30		40	ns	2
t_{OH}	t_{AXQX}	Output Hold From Address Change	5		5		ns	1

Figure 3. READ TIMING NO. 1 (ADDRESS ACCESS)

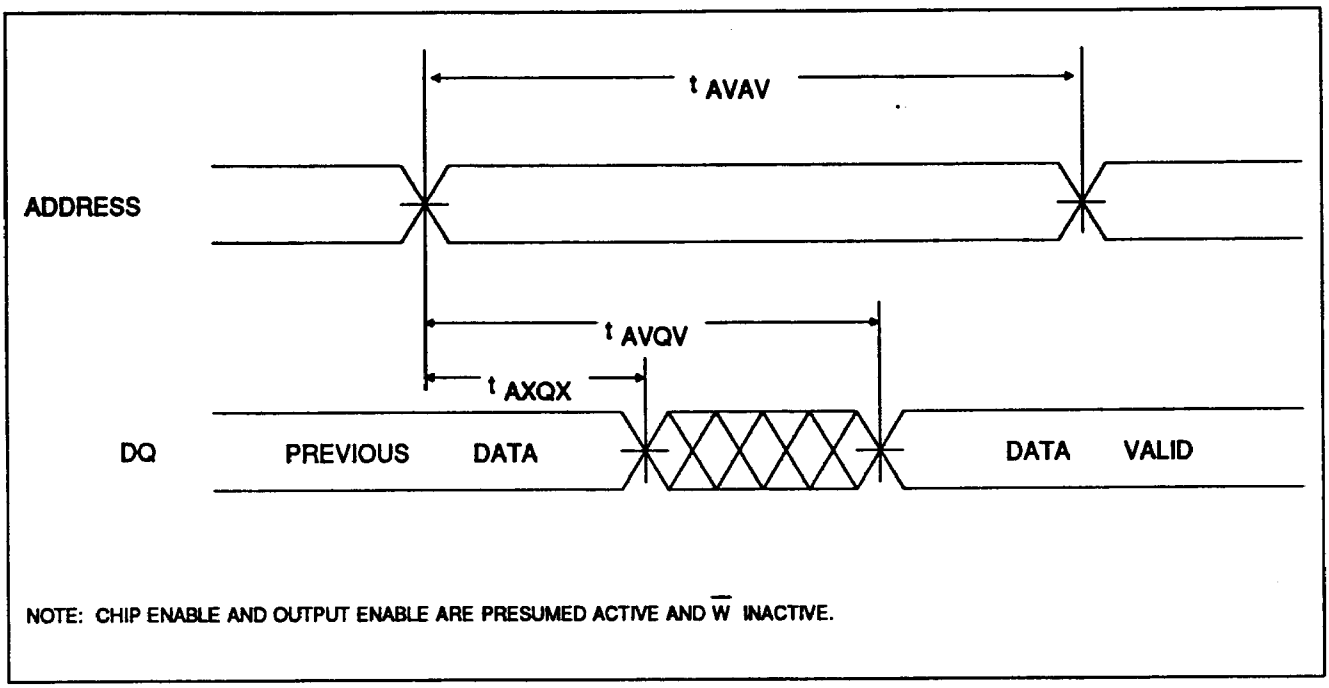
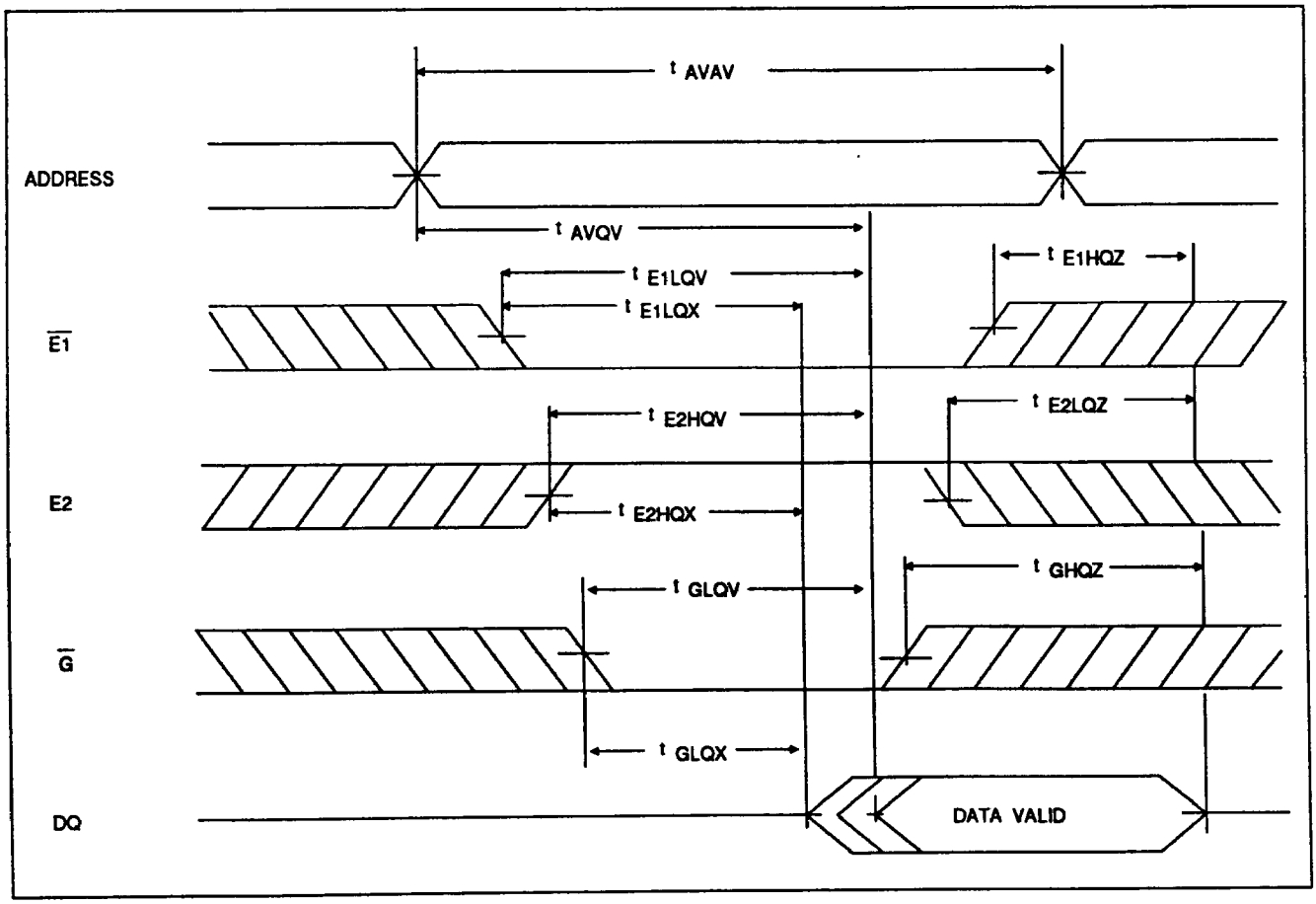


Figure 4. READ TIMING NO. 2 ($\overline{W}$ = V_{IH})



WRITE MODE

The MK6264 is in the Write mode whenever the $\overline{W}$ and $\overline{E1}$ pins are low, with E2 high. Either Chip Enable pin or $\overline{W}$ must be inactive during Address transitions. The Write begins with the concurrence of both Chip Enables being active with $\overline{W}$ low. Therefore, address setup times are referenced to Write Enable and both Chip Enables as t_{AVWL}, t_{AVE1L} and t_{AVE2H} respectively, and is determined to the latter occuring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E1}$ or $\overline{W}$, or the falling edge of E2.

If the Output is enabled ($\overline{E1}$ = low, E2 = high, $\overline{G}$ = low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{E1}$, or the falling edge of E2, whichever occurs first, and remain valid t_{WHDX} after the rising edge of $\overline{E1}$ or $\overline{W}$, or the falling edge of E2.

WRITE CYCLE TIMING

{0° C ≤ T_A ≤ 70° C , Vcc = 5.0 V ± 10 %}

SYMBOLS		PARAMETERS	MK6264-70 MK6264L-70 MK6264U-70		MK6264-120 MK6264L-120 MK6264U-120			
ALT.	STD.		MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	t_{AVAV}	Write Cycle Time	70		120		ns	
t_{AS}	t_{AVWL}	Address Set-up Time to Write Enable Low	0		0		ns	
t_{AS}	t_{AVE1L} t_{AVE2H}	Address Set-up Time to Chip Enable	0		0		ns	
t_{AW}	t_{AVWH}	Address Valid to End of Write	60		85		ns	
t_{WEW}	t_{WLWH}	Write Pulse Width	60		70		ns	
t_{AH}	t_{WHAX}	Address Hold Time after End of Write	0		0		ns	
t_{CEW}	t_{E1LE1H} t_{E2HE2L}	Chip Enable to End of Write	60		70		ns	
t_{WR}	t_{E1HAX} t_{E2LAX}	Write Recovery Time to Chip Disable	0		0		ns	
t_{DW}	t_{DVWH}	Data Valid to End of Write	40		40		ns	
t_{DH}	t_{WHDX}	Data Hold Time	0		0		ns	
t_{WEL}	t_{WHQX}	Write High to Output Low-Z (Active)	0		0		ns	2
t_{WEZ}	t_{WLQZ}	Write Enable to Output High-Z		30		35	ns	2

Figure 5. WRITE TIMING NO. 1 ($\overline{W}$ CONTROL)

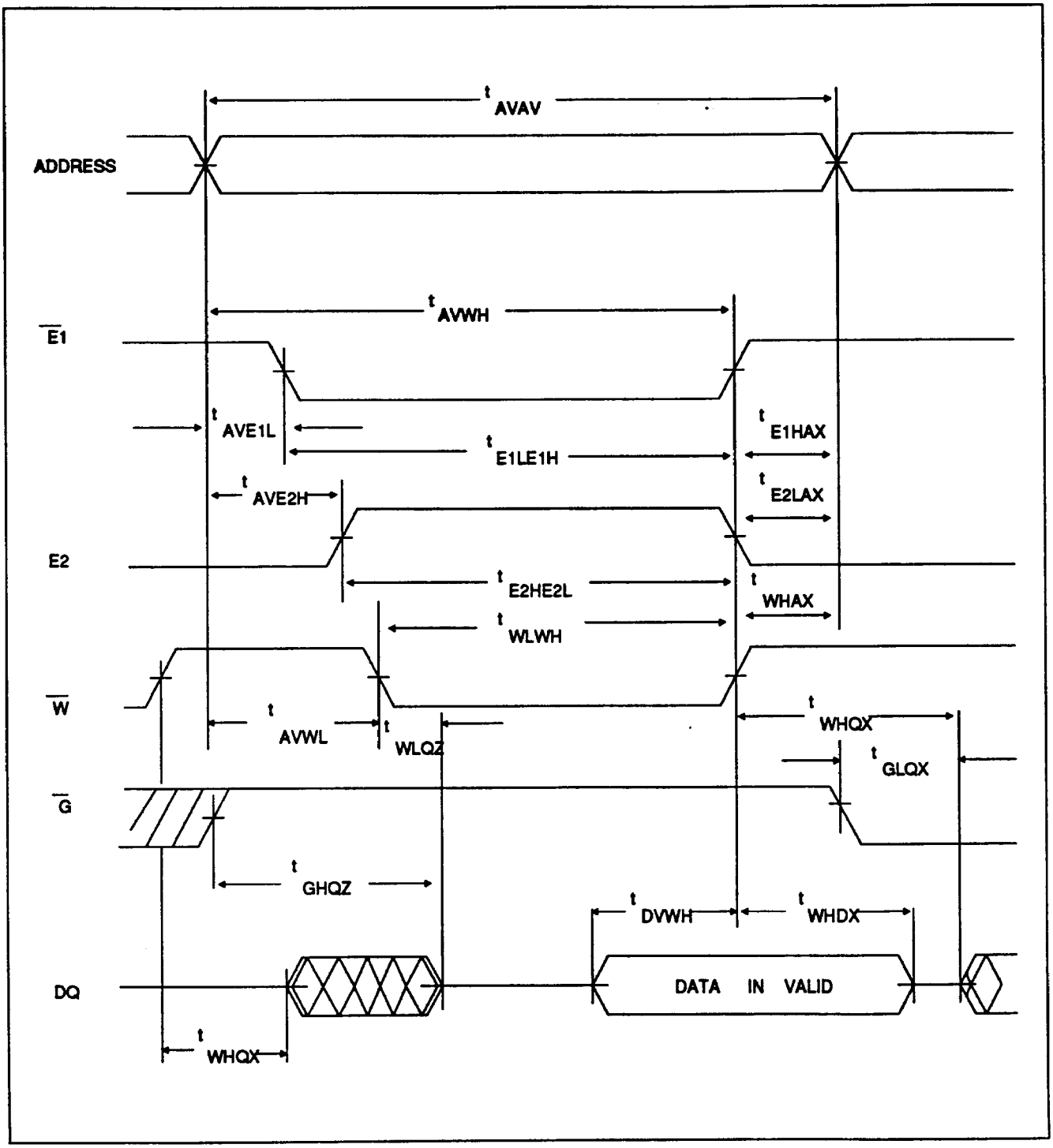
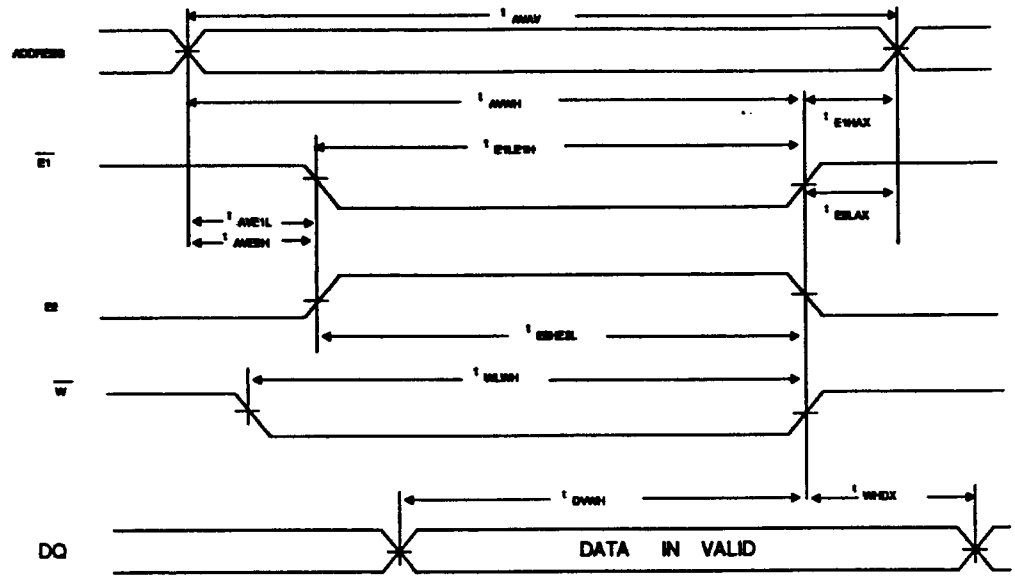


Figure 6. WRITE TIMING NO. 2 ($\overline{E1}$ CONTROL)



NOTE: $\overline{G}$ = V_{IH}.

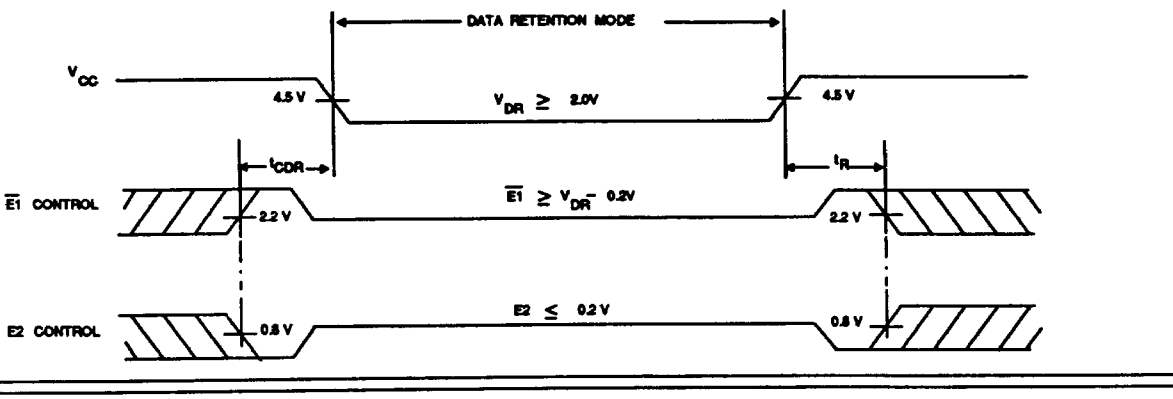
LOW Vcc DATA RETENTION CHARACTERISTICS

{0° C ≤ T_A ≤ 70° C}

SYMBOLS	PARAMETERS	MIN	MAX	UNIT	NOTES
VDR	Vcc Data Retention	2.0	Vcc(min)	V	
IccDR	Data Retention Pwr. Supply Current, MK6264 MK6264L MK6264U		500 25 2	µA µA µA	3
tCDR	Chip Deselection to Data Retention Time	0		ns	
tR	Operation Recovery Time	tAVAV*		ns	

* tAVAV = READ CYCLE TIME

Figure 7. LOW Vcc DATA RETENTION TIMING



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to GND. . . . . -1.0 V to 7.0 V
Ambient Operating Temperature (T_A). . . . . 0° C to 70° C
Ambient Storage Temperature (Plastic). . . . . -55° C to 125° C
Total Device Power Dissipation. . . . . 1 Watt
Output Current per Pin. . . . . 50 mA

Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

{0 ° C ≤ T_A ≤ 70 ° C }

SYMBOLS	PARAMETERS	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	4
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.2		Vcc+0.3	V	4
V_{IL}	Logic 0 Voltage, All Inputs	-0.3		0.8	V	4

DC ELECTRICAL CHARACTERISTICS

{0° C ≤ T_A ≤ 70° C , Vcc = 5.0 V ± 10 %}

SYMBOLS	PARAMETERS		MIN	MAX	UNITS	NOTES
I_{CC}	Average Power Supply Current, f = min cycle			45	mA	5
I_{SB1}	TTL Standby Current			7	mA	6
I_{SB2}	CMOS Standby Current,	MK6264 MK6264L MK6264U		1 50 10	mA µA µA	7
I_{LI}	Input Leakage Current (Any Input Pin)		-1	+1	µA	8
I_{LO}	Output Leakage Current (Any Output Pin)		-2	+2	µA	9
V_{OH}	Output Logic 1 Voltage (I_{OH} = -4 mA)		2.4		V	4
V_{OL}	Output Logic 0 Voltage (I_{OL} = 8 mA)			0.4	V	4

CAPACITANCE

(T_A = 25° C, f = 1.0 MHz)

SYMBOLS	PARAMETERS	TYP	MAX	UNITS	NOTES
C_1	Capacitance on input pins	4	5	pF	10
C_2	Capacitance on DQ pins	8	10	pF	10

NOTES:

1. Measured with load shown in Figure 8(A).
2. Measured with load shown in Figure 8(B).
3. VCC = 3.0V
4. All voltages referenced to GND.
5. ICC1 is measured as the average AC current with VCC = VCC (max) and with the outputs open circuit. t_{AVAV} = t_{AVAV} (min) duty cycle 100%.
6. $\overline{E1}$ = VIH, all other Inputs = Don't Care.
7. VCC (max), and E2 ≤ VSS + 0.3 V, all other Inputs = Don't Care.
8. Input leakage current specifications are valid for all VIN such that 0 V < VIN < VCC. Measured at VCC = VCC (max).
9. Output leakage current specifications are valid for all VOUT such that 0 V < VOUT < VCC, $\overline{E1}$ = VIH or E2 = VIL, and VCC in valid operating range.
10. Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

Input Levels. . . . . GND to 3.0 V
Transition Times. . . . . .5 ns
Input and Output Signal Timing Reference Level. . . . . 1.5 V
Ambient Temperature. . . . . 0° C to 70° C
Vcc. . . . . 5.0 V ± 10 %

Figure 8. OUTPUT LOAD CIRCUITS

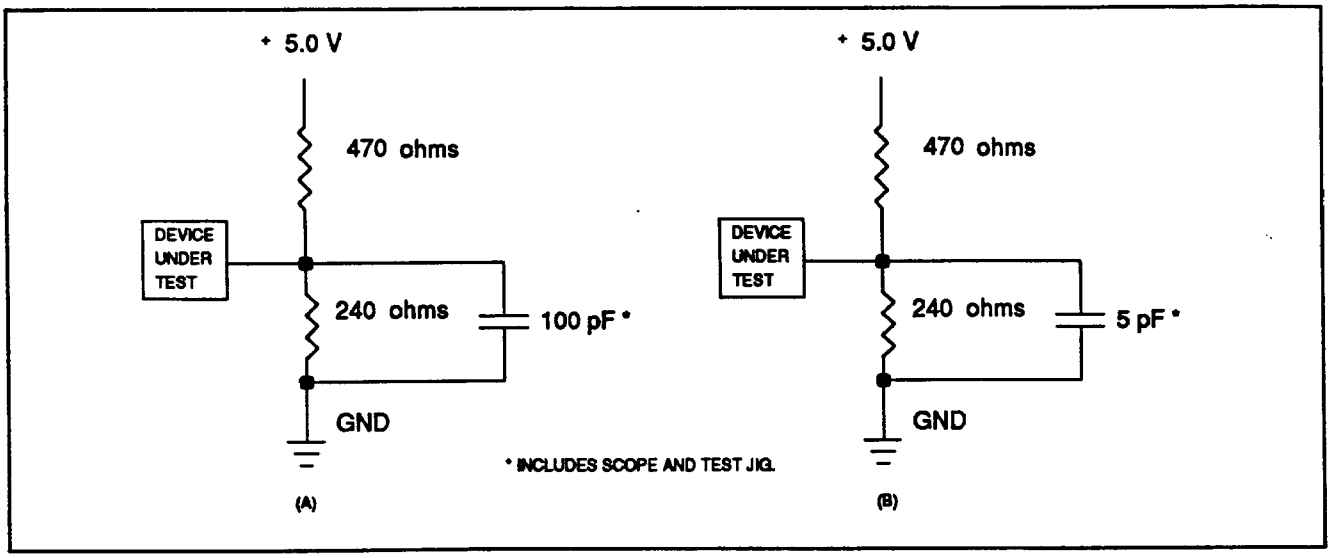
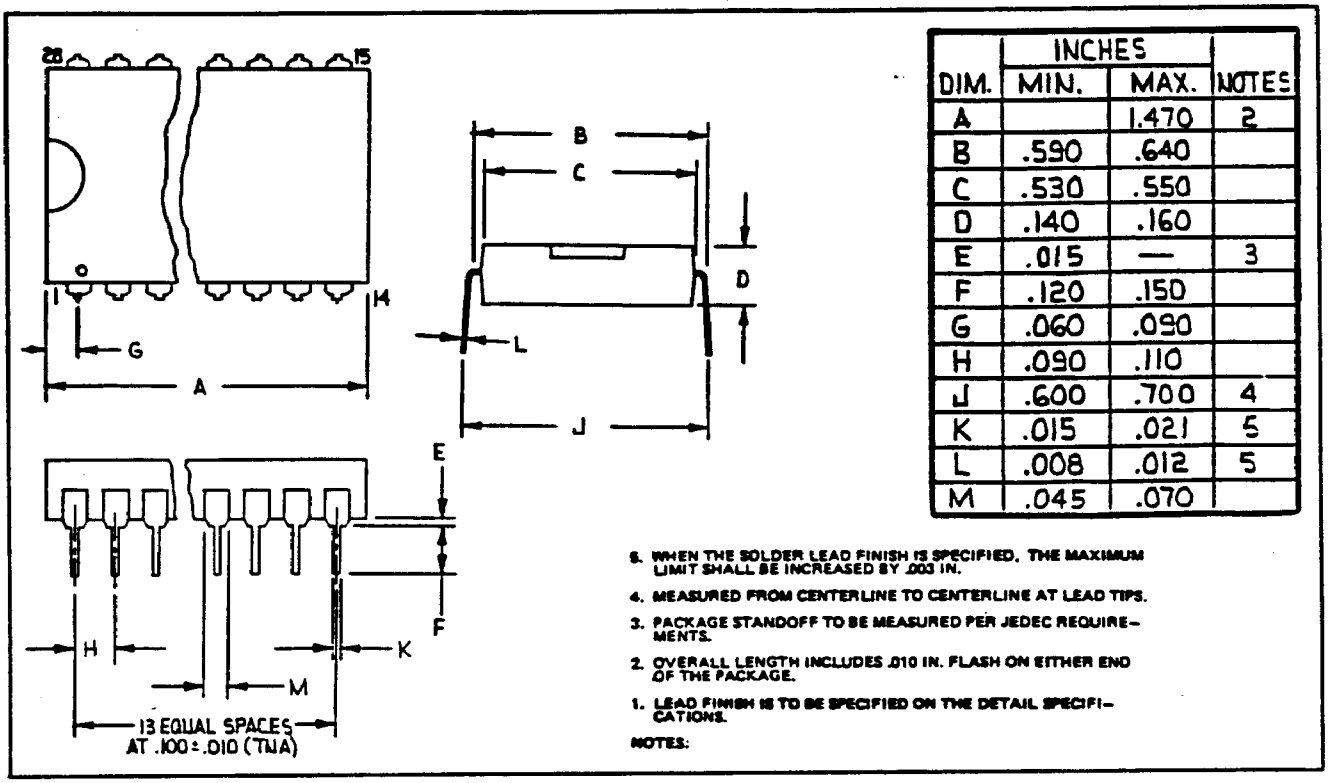


Figure 9. 28-PIN PLASTIC DIP (N)

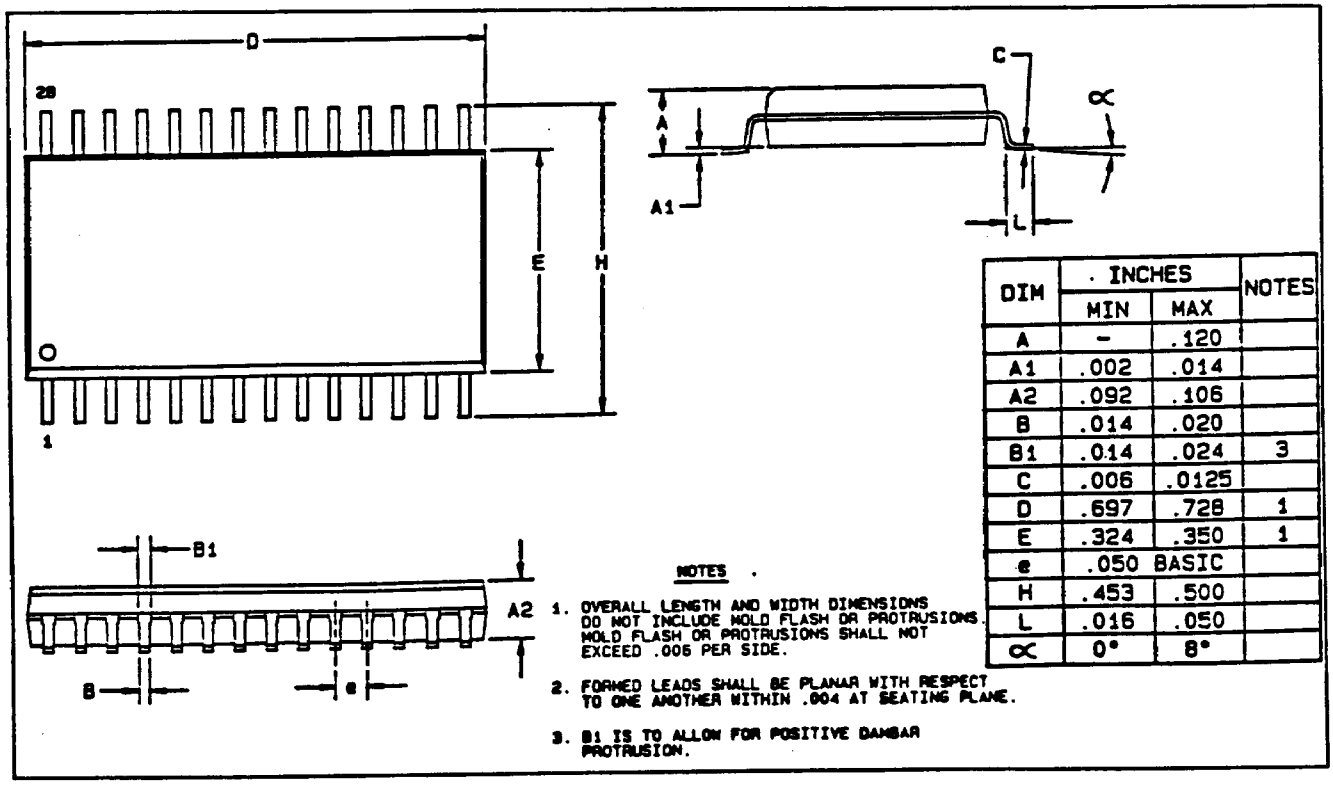


DIM.	INCHES MIN.	INCHES MAX.	NOTES
A		1.470	2
B	.590	.640	
C	.530	.550	
D	.140	.160	
E	.015	—	3
F	.120	.150	
G	.060	.090	
H	.090	.110	
J	.600	.700	4
K	.015	.021	5
L	.008	.012	5
M	.045	.070	

NOTES:

1. LEAD FINISH IS TO BE SPECIFIED ON THE DETAIL SPECIFICATIONS.
2. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
3. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
4. MEASURED FROM CENTERLINE TO CENTERLINE AT LEAD TIPS.
5. WHEN THE SOLDER LEAD FINISH IS SPECIFIED, THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN.

Figure 10. 28-PIN SOIC (S)



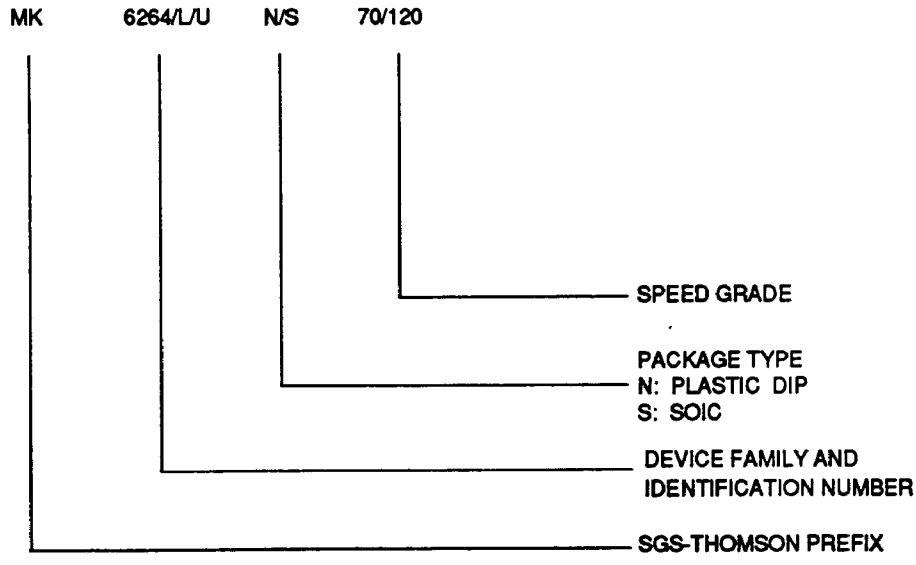
DIM	INCHES MIN	INCHES MAX	NOTES
A	–	.120	
A1	.002	.014	
A2	.092	.106	
B	.014	.020	
B1	.014	.024	3
C	.006	.0125	
D	.697	.728	1
E	.324	.350	1
e	.050 BASIC		
H	.453	.500	
L	.016	.050	
∝	0°	8°	

NOTES

1. OVERALL LENGTH AND WIDTH DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 PER SIDE.
2. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004 AT SEATING PLANE.
3. B1 IS TO ALLOW FOR POSITIVE DAMBAR PROTRUSION.

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK6264(N/S)-70	70ns	600 mil Plastic DIP/ 330 mil SOIC	0° C to 70° C
MK6264(N/S)-120	120ns	600 mil Plastic DIP/ 330 mil SOIC	0° C to 70° C
MK6264L(N/S)-70	70ns	600 mil Plastic DIP/ 330 mil SOIC	0° C to 70° C
MK6264L(N/S)-120	120ns	600 mil Plastic DIP/ 330 mil SOIC	0° C to 70° C
MK6264U(N/S)-70	70ns	600 mil Plastic DIP/ 330 mil SOIC	0° C to 70° C
MK6264U(N/S)-120	120ns	600 mil Plastic DIP/ 330 mil SOIC	0° C to 70° C



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