2048-BIT STATIC RAM WITH I/O PORTS AND TIMER

DESCRIPTION

The M5L8155P is a 2K-bit RAM (256-word by 8-bit) fabricated by the N-channel silicon-gate ED-MOS technology. This LSI has 3 I/O ports and a 14-bit counter/timer which make it a good extention of the functions of an 8-bit microcomputer. It is packaged in a 40-pin plastic DIL package and operates with a single 5V power supply.

FEATURES

- Single 5V supply voltage
- TTL compatible
- Static RAM: 256-word by 8-bit
- Programmable 8-bit I/O port: 2
- Programmable 6-bit I/O port: 1
- Programmable counter/timer: 14-bit
- Multiplexed address/data bus

APPLICATION

Extension of I/O ports and timer function for MELPS 85 and MELPS 8-48 devices

FUNCTION

The M5L8155P is composed of RAM, I/O ports and counter/timer. The RAM is a 2K-bit static RAM organized as 256 words by 8 bits. The I/O ports consist of 2 programmable 8-bit ports and 1 programmable 6-bit port. The terminals of the 6-bit port can be programmed as control terminals for the 8-bit ports, so that the 8-bit ports can be operated in a handshake mode. The counter/timer is composed of 14-bit down counter (events or time) and it can generate square wave pulses that can be used for counting and timing.

PIN CONFIGURATION (TOP VIEW)

Pin	Signal		Pin	Signal
I/O PORTS C	PC$_3$ ←→ 1		40	V$_{CC}$(5V)
	PC$_4$ ←→ 2		39	←→ PC$_2$
TIMER INPUT TIMER IN →	3		38	←→ PC$_1$ (I/O PORTS C)
RESET INPUT RESET →	4		37	←→ PC$_0$
I/O PORT C	PC$_5$ ←→ 5		36	←→ PB$_7$
TIMER OUTPUT TIMER OUT ←	6		35	←→ PB$_6$
IO/MEMORY SELECT INPUT IO/$\overline{M}$ →	7		34	←→ PB$_5$
CHIP ENABLE INPUT $\overline{CE}$ →	8		33	←→ PB$_4$ (I/O PORTS B)
READ INPUT $\overline{RD}$ →	9		32	←→ PB$_3$
WRITE INPUT $\overline{WR}$ →	10		31	←→ PB$_2$
ADDRESS LATCH ENABLE INPUT ALE →	11		30	←→ PB$_1$
	AD$_0$ ←→ 12		29	←→ PB$_0$
	AD$_1$ ←→ 13		28	←→ PA$_7$
	AD$_2$ ←→ 14		27	←→ PA$_6$
BIDIRECTIONAL ADDRESS/DATA BUS	AD$_3$ ←→ 15		26	←→ PA$_5$
	AD$_4$ ←→ 16		25	←→ PA$_4$ (I/O PORTS A)
	AD$_5$ ←→ 17		24	←→ PA$_3$
	AD$_6$ ←→ 18		23	←→ PA$_2$
	AD$_7$ ←→ 19		22	←→ PA$_1$
	(0V)V$_{SS}$ 20		21	←→ PA$_0$

Outline 40P4

BLOCK DIAGRAM

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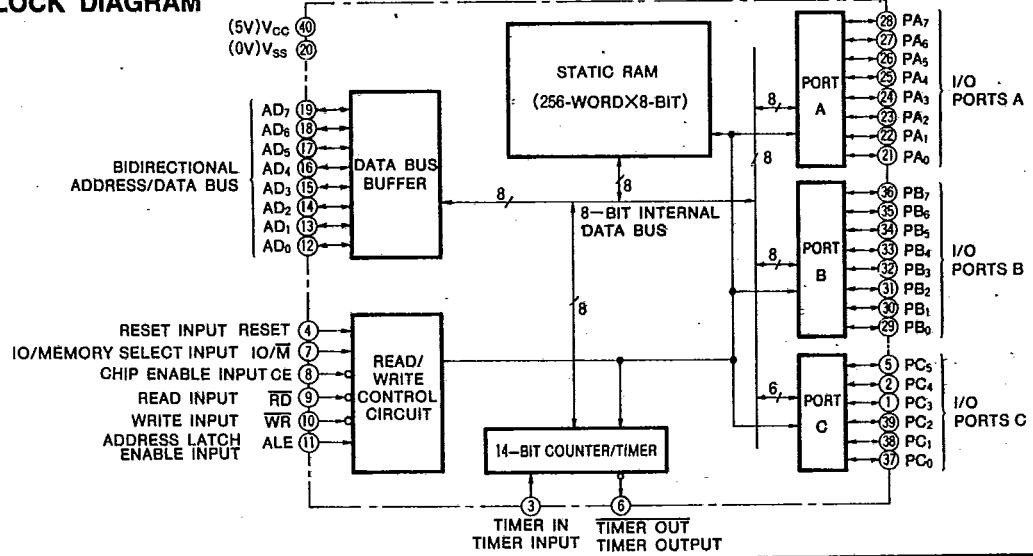
OPERATION

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to transfer the data while input or output instructions are being executed by the CPU. Command and address information is also transferred through the data bus buffer.

Read/Write Control Logic

The read/write control logic controls the transfer of data and commands by interpreting the signals ($\overline{CE}$, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, ALE and RESET) from CPU.

Bidirectional Address/Data Bus (AD$_0$~AD$_7$)

The bidirectional address/data bus is a 3-state 8-bit bus. The 8-bit address is latched in the internal latch by the falling edge of ALE. Then if IO/$\overline{M}$ input signal is at high-level, the address of I/O port, counter/timer, or command register is selected. If it is at low-level, address of RAM is selected. The 8-bit data is transferred by read input ($\overline{RD}$) or write input ($\overline{WR}$).

Chip Enable Input ($\overline{CE}$)

When $\overline{CE}$ is at low-level, the address information on address/data bus is stored in the M5L8155P.

Read Input ($\overline{RD}$)

When $\overline{RD}$ is at low-level, the data bus buffer is active. If IO/$\overline{M}$ input signal is at low-level, the contents of RAM are read through the address/data bus. If IO/$\overline{M}$ input is at high-level, the contents of selected I/O port or counter/timer are read through the address/data bus.

Write Input ($\overline{WR}$)

When $\overline{WR}$ is at low-level, the data on the address/data bus are written into RAM if IO/$\overline{M}$ is at low-level, or they are written into I/O port, counter/timer or command register if IO/$\overline{M}$ is at high-level.

Address Latch Enable Input (ALE)

An address on the address/data bus is latched in the M5L8155P on the falling edge of ALE along with the levels of $\overline{CE}$ and IO/$\overline{M}$.

IO/Memory Input (IO/$\overline{M}$)

When IO/$\overline{M}$ is at low-level, the RAM is selected, while at high-level the I/O port, counter/timer or command register are selected.

I/O Port A (PA$_0$~PA$_7$)

Port A is an 8-bit general-purpose I/O port. Input/output setting is controlled by the system software.

I/O Port B (PB$_0$~PB$_7$)

Port B is an 8-bit general-purpose I/O port. Input/output setting is controlled by the system software.

I/O Port C (PC$_0$~PC$_5$)

Port C is a 6-bit I/O port that can also be used to output control signals of port A (PA) or port B (PB). The functions of port C are controlled by the system software. When port C is used to output control signals of ports A or B, the assignment of the signals to the pins is as shown in Table 1.

Table 1 Pin assignment of control signals of port C

Pin	Function	
PC$_5$	$\overline{B\ STB}$	(port B strobe)
PC$_4$	B BF	(port B buffer full)
PC$_3$	B INTR	(port B interrupt)
PC$_2$	$\overline{A\ STB}$	(port A strobe)
PC$_1$	A BF	(port A buffer full)
PC$_0$	A INTR	(port A interrupt)

Timer Input (TIMER IN)

The signal on this input terminal is used by the counter/timer for counting events or time. (3MHz max.)

Timer Output ($\overline{TIMER\ OUT}$)

A square wave signal or pulse from the counter/timer is output through this pin when in the operation mode.

Command Register (8 bits)

The command register is an 8-bit latched register. The low-order 4 bits (bits 0~3) are used for controlling and determination of mode of the ports. Bits 4 and 5 are used as interrupt enable flags for ports A and B when port C is used as a control port. Bits 6 and 7 are used for controlling the counter/timer. The contents of the command register are rewritten by output instructions (I/O address XXXXX000).

Details of the functions of the individual bits of the command register are shown in Table 2.

Table 2 Bit functions of the command register

Bit	Symbol	Function	
0	PA	PORT A I/O SET	1: Output port A 0: Input port A
1	PB	PORT B I/O SET	1: Output port B 0: Input port B
2	PC$_1$	PORT C SET	00: ALT1 11: ALT2
3	PC$_2$		01: ALT3 10: ALT4
4	IEA	PORT A INTERRUPT ENABLE FLAG	1: Enable interrupt 0: Disable interrupt
5	IEB	PORT B INTERRUPT ENABLE FLAG	1: Enable interrupt 0: Disable interrupt
6	TM1	COUNTER/TIMER CONTROL 00: No influence on counter/timer operation 01: Counter/timer operation discontinued (if not already stopped)	
7	TM2	10: Counter/timer operation discontinued after the current counter/timer operation is completed 11: Counter/timer operation started	

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Status Register (7-bit)

The status register is a 7-bit latched register. The low-order 6 bits (bits 0~5) are used as status flags for the I/O ports. Bit 6 is used as a status flag for the counter/timer. The contents of the status register are transferred into the CPU by reading (INPUT instruction, I/O address XXXXX000). Details of the functions of the individual bits of the status register are shown in Table 3.

Table 3 Bit functions of the status register

Bit	Symbol	Function
0	INTR A	PORT A INTERRUPT REQUEST
1	A BF	PORT A BUFFER FULL FLAG
2	INTE A	PORT A INTERRUPT ENABLE
3	INTR B	PORT B INTERRUPT REQUEST
4	B BF	PORT B BUFFER FULL FLAG
5	INTE B	PORT B INTERRUPT ENABLE
6	TIMER	COUNTER/TIMER INTERRUPT — This flag is set to 1 when the final limit of the counter/timer is reached and is reset to 0 when the status is read
7	—	This bit is not used

I/O PORTS

Command/status registers (8-bit/7-bit)

These registers are assigned address XXXXX000. When an OUTPUT command is executed, the contents of the command register are rewritten. When an INPUT command is executed, the contents of the status register are read.

Port A Register (8-bit)

Port A Register is assigned address XXXXX001. This register can be programmed as an input or output by setting the appropriate bits of the command register as shown in Table 2.

Port A can be operated in basic or strobe mode and is assigned I/O terminal $PA_0 \sim PA_7$.

Port B Register (8-bit)

Port B register is assigned address XXXXX010. As with Port A register, this register can be programmed as an input or output by setting the appropriate bits of the command register as shown in Table 2. Port B can be operated in basic or strobe mode and is assigned I/O terminals $PB_0 \sim PB_7$.

Port C Register (6-bit)

Port C register is assigned address XXXXX011. This port is used not only for input or output but also for controlling input/output operations of ports A and B by selectively setting bits 2 and 3 of the command register as shown in Table 2. Details of the functions of the various setting of bits 2 and 3 are shown in Table 4. Port C is assigned I/O terminals $PC_0 \sim PC_5$. When used as port control signals, the 3 low-order bits are assigned for port A while the 3 high-order bits are assigned for port B.

Table 4 Functions of port C

State Terminal	ALT 1	ALT 2	ALT 3	ALT 4
PC_5	Input	Output	Output	B STB (port B strobe)
PC_4	Input	Output	Output	B BF (port B buffer full)
PC_3	Input	Output	Output	B INTR (port B interrupt)
PC_2	Input	Output	$\overline{\text{A STB}}$ (port A strobe)	$\overline{\text{A STB}}$ (port A strobe)
PC_1	Input	Output	A BF (port A buffer full)	A BF (port A buffer full)
PC_0	Input	Output	A INTR (port A interrupt)	A INTR (port A interrupt)

2048-BIT STATIC RAM WITH I/O PORTS AND TIMER

CONFIGURATION OF PORTS

A block diagram of 1 bit of ports A and B is shown in Fig. 1. While port A or B is programmed as an output port, if the port is addressed by an input instruction, the contents of the selected port can be read. When a port is put in input mode, the output latch is cleared and writing into the output latch is disabled. Therefore when a port is changed to output mode from input mode, low-level signals are output through the port. When a reset signal is applied, all 3 ports (PA, PB, and PC) will be input ports and their output latches are cleared. Port C has the same configuration as ports A and B in modes ALT1 and ALT2.


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Note 1. WR PORT=IO/$\overline{M}$·WR·CE
(PORT ADDRESS SELECTED)
2. RD PORT=IO/$\overline{M}$·RD·CE
(PORT ADDRESS SELECTED)
3. MULTIPLEX CONTROL
 *1 STROBE INPUT MODE
 *2 INPUT MODE
 *3 OUTPUT MODE
4. MD=1 : OUTPUT MODE
 0 : INPUT MODE
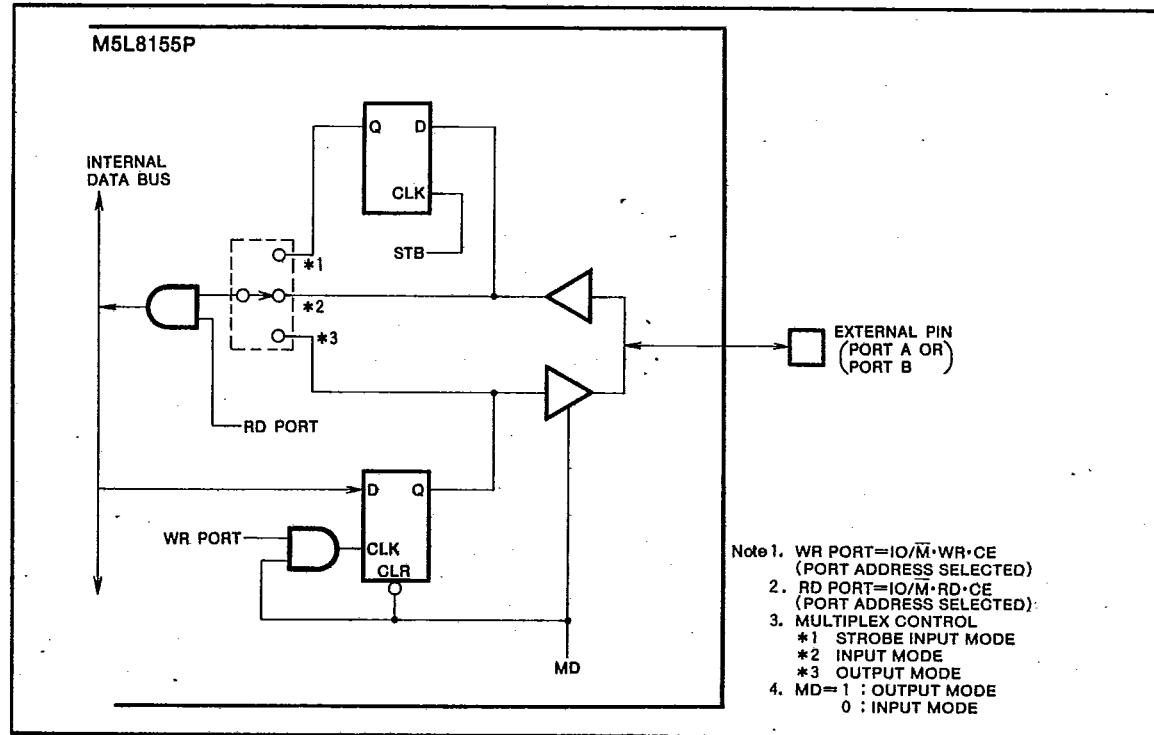
Fig. 1 Configuration for 1 bit of port A or B

Table 5 Basic functions of I/O ports

Address	RD	WR	Function
XXXXX000	L	H	AD bus ← Status register
	H	L	Command register ← AD bus
XXXXX001	L	H	AD bus ← Port A
	H	L	Port A ← AD bus
XXXXX010	L	H	AD bus ← Port B
	H	L	Port B ← AD bus
XXXXX011	L	H	AD bus ← Port C
	H	L	Port C ← AD bus

Table 6 Port control signal levels at ALT3 and ALT4

Control Signal	Output mode	Input mode
STB	Input	Input
BF	"L"	"L"
INTR	"H"	"L"

The basic functions of the I/O ports are shown in Table 5. The control signal levels to ports A and B, when port C is programmed as a control port, are shown in Table 6.

COUNTER/TIMER

The counter/timer is composed of a 14-bit counting register and 2 mode flags. The register has two sections: I/O address XXXXX100 is assigned to the low-order 8 bits and I/O address XXXXX101 is assigned to the high-order 6 bits and timer mode flag 2 bits. The low-order bits 0~13 are used for counting or timing. The counter is initialized by the program and then counted down to 0. The initial value can be ranged from 2_{16} to $3FFF_{16}$. Bits 14 and 15 are used as mode flags.

The mode flags select 1 of 4 modes with functions as follows:

Mode 0: Outputs high-level signal during the former half of the counter operation
Outputs low-level signal during the latter half of the counter operation

2048-BIT STATIC RAM WITH I/O PORTS AND TIMER

Table 7 Format of counter/timer

Address	Bit Number								Function
	7	6	5	4	3	2	1	0	
XXXXX100	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0	The low-order 8 bits of the counter register
XXXXX101	M_2	M_1	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	M2,M1: Timer mode $T_{13} \sim T_8$: The high-order 6 bits of the counter register

Table 8 Timer mode

M_2	M_1	Timer operation
0	0	Outputs high-level signal during the former half of the counter operation Outputs low-level signal during the latter half of the counter operation (mode 0)
0	1	Outputs square wave signals in mode 0 (mode 1)
1	0	Outputs a low-level pulse during the final count down (mode 2)
1	1	Outputs a low-level pulse during each final count down (mode 3)

Mode 1: Outputs square wave signals as in mode 0
Mode 2: Outputs a low-level pulse during the final count down
Mode 3: Outputs a low-level pulse during each final count down

Starting and stopping the counter/timer is controlled by bits 6 and 7 of the command register (see Table 2 for details). The format and timer modes of the counter/timer register are shown in Table 7 and Table 8.

The contents of counter/timer is not affected by a reset, but counting is discontinued. To resume counting, a start command must be written into the command register as shown in Table 2. While operating $2n+1$ count down in modes 0 and 1, a high-level signal is output during the former $n+1$ counting and a low-level signal is output during the later n counting.

RESET

The M5L8155P is reset by 600ns (min) pulse input on RESET pin.
By reset, all 3 ports are set to input mode. And counter/timer stops, but contents of counter/timer is not reset. Therefore it is necessary to input start command again.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	$-0.5 \sim 7$	V
V_I	Input voltage		$-0.5 \sim 7$	V
V_O	Output voltage		$-0.5 \sim 7$	V
P_d	Maximum power dissipation	$T_a = 25°C$	1.5	W
T_{opr}	Operating free-air temperature range		$-20 \sim 75$	°C
T_{stg}	Storage temperature range		$-65 \sim 150$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim 75°C$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Power-supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim 75°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		$V_{CC}+0.5$	V
V_{IL}	Low-level input voltage		-0.5		0.8	V
V_{OH}	High-level output voltage	$I_{OH} = -400\mu A$	2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 2mA$			0.45	V
I_I	Input leak current	$V_I = 0V$, V_{CC}	-10		10	μA
$I_{I(CE)}$	Input leak current, CE pin	$V_I = 0V$, V_{CC}	-100		100	μA
I_{OZ}	Output floating leak current	$V_O = 0V \sim V_{CC}$	-10		10	μA
C_I	Input terminal capacitance	$V_{IL} = 0V$, $f = 1MHz$, 25mVrms, $T_a = 25°C$			10	pF
$C_{I/O}$	Input/output terminal capacitance	$V_{I/OL} = 0V$, $f = 1MHz$, 25mVrms, $T_a = 25°C$			20	pF
I_{CC}	Supply current from V_{CC}				180	mA

Note 5 : Current flowing into an IC is positive, out is negative.

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TIMING REQUIREMENTS (Ta=−20~75℃, Vcc=5V±5%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{SU(A-L)}$	Address setup time before latch		50			ns
$t_{h(L-A)}$	Address hold time after latch		80			ns
$t_{d(L-RW)}$	Delay time, latch to read/write		100			ns
$t_{W(L)}$	Latch pulse width		100			ns
$t_{d(RW-L)}$	Delay time, read/write to latch		20			ns
$t_{W(RW)}$	Read/write pulse width		250			ns
$t_{SU(DQ-W)}$	Data setup time before write		150			ns
$t_{h(W-DQ)}$	Data hold time after write		0			ns
$t_{C(RW)}$	Read/write cycle time		300			ns
$t_{SU(P-R)}$	Port setup time before read		70			ns
$t_{h(R-P)}$	Port hold time after read		50			ns
$t_{W(STB)}$	Strobe pulse width		200			ns
$t_{SU(P-STB)}$	Port setup time before strobe		50			ns
$t_{h(STB-P)}$	Port hold time after strobe		120			ns
$t_{W(\neq H)}$	Timer input high-level pulse width		120			ns
$t_{W(\neq L)}$	Timer input low-level pulse width		80			ns
$t_{C(\neq)}$	Timer input cycle time		320		DC	ns
$t_{r(\neq)}$	Timer input rise time				30	ns
$t_{f(\neq)}$	Timer input fall time				30	ns

SWITCHING CHARACTERISTICS (Ta=−20~75℃, Vcc=5V±5%, Vss=0V, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{PZV(R-DQ)}$	Propagation time from read to data output				170	ns
$t_{PZV(A-DQ)}$	Propagation time from address to data output				400	ns
$t_{PVZ(R-DQ)}$	Propagation time from read to data floating (Note 6)		0		100	ns
$t_{PHL(W-P)}$ $t_{PLH(W-P)}$	Propagation time from write to data output				400	ns
$t_{PLH(STB-BF)}$	Propagation time from strobe to BF flag				400	ns
$t_{PHL(R-BF)}$	Propagation time from read to BF flag	$C_L = 150pF$			400	ns
$t_{PLH(STB-INTR)}$	Propagation time from strobe to interrupt				400	ns
$t_{PHL(R-INTR)}$	Propagation time from read to interrupt				400	ns
$t_{PHL(STB-BF)}$	Propagation time from strobe to BF flag				400	ns
$t_{PLH(W-BF)}$	Propagation time from write to BF flag				400	ns
$t_{PHL(W-INTR)}$	Propagation time from write to interrupt				400	ns
$t_{PHL(\neq-OUT)}$ $t_{PLH(\neq-OUT)}$	Propagation time from timer input to timer output				400	ns

Note 6 : Test conditions are not applied.
    7 : A.C Testing waveform
      Input pulse level   0.45~2.4V
      Input pulse rise time 20ns
      Input pulse fall time 20ns
      Reference level input $V_{IH}=2V$, $V_{IL}=0.8V$
              output $V_{OH}=2V$, $V_{OL}=0.8V$

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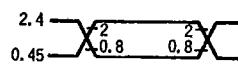
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2048-BIT STATIC RAM WITH I/O PORTS AND TIMER

TIMING DIAGRAM

Basic Output
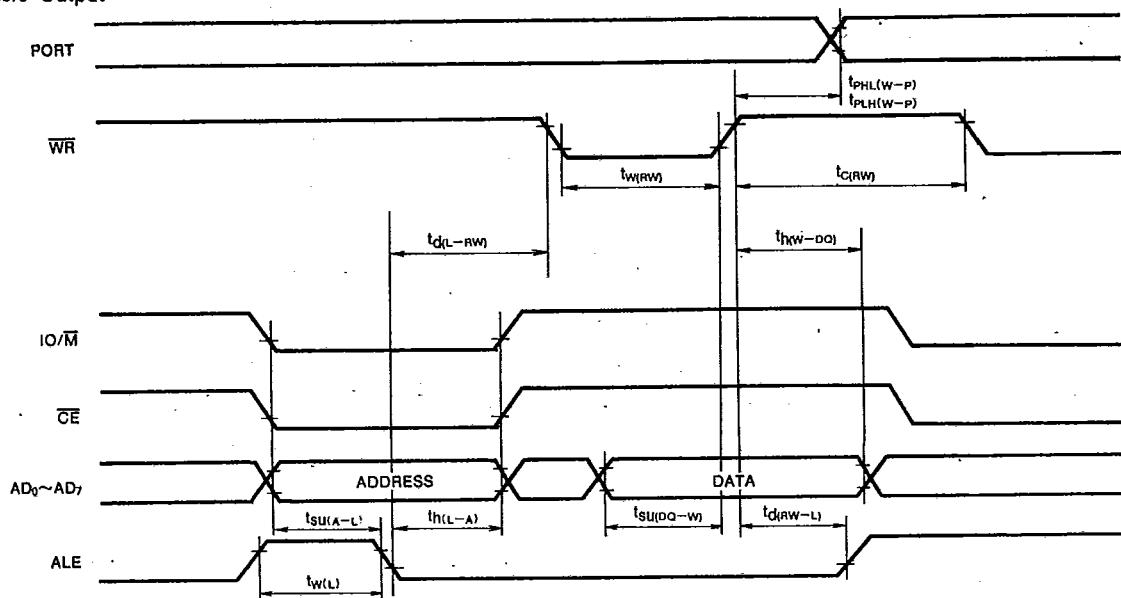
Basic Input

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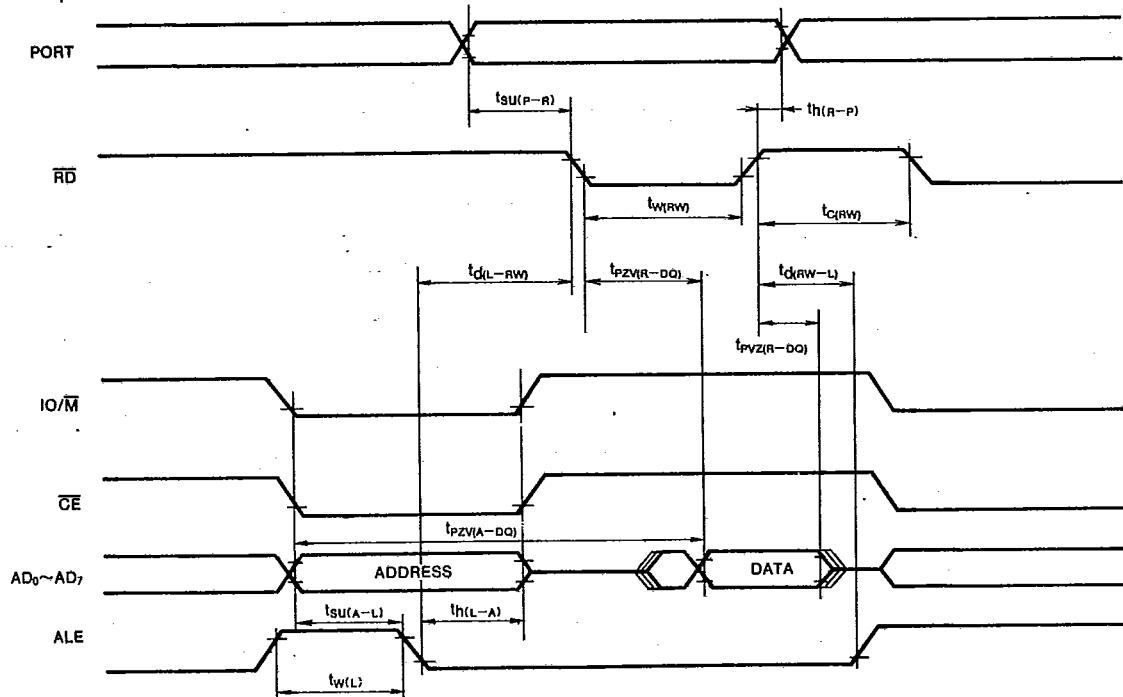
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2048-BIT STATIC RAM WITH I/O PORTS AND TIMER

Strobed Output

PORT

$t_{PLH(W-P)}$
$t_{PHL(W-P)}$

$\overline{WR}$

$t_{PHL(W-INTR)}$

INTR

$t_{PLH(W-BF)}$

$t_{PLH(STB-INTR)}$

BF

$t_{PHL(STB-BF)}$

$\overline{STB}$

Strobed Input

PORT

$t_{SU(P-STB)}$ $t_{h(STB-P)}$

$\overline{STB}$

$t_{W(STB)}$ $t_{PLH(STB-INTR)}$

$t_{PLH(STB-BF)}$

BF

$t_{PHL(R-BF)}$

INTR

$t_{PHL(R-INTR)}$

$\overline{RD}$

Timer

(Note 8)

TIMER IN   1   5   4   3   2   1   5

$t_{W(\neq L)}$ $t_{W(\neq H)}$ $t_{r(\neq)}$ $t_{f(\neq)}$

$t_{C(\neq)}$

$\overline{TIMER\ OUT}$
PULSE MODE   (Note 9)

$t_{PHL(\neq-OUT)}$

$t_{PHL(\neq-OUT)}$ $t_{PLH(\neq-OUT)}$

$\overline{TIMER\ OUT}$
SQUARE WAVE MODE   (Note 9)
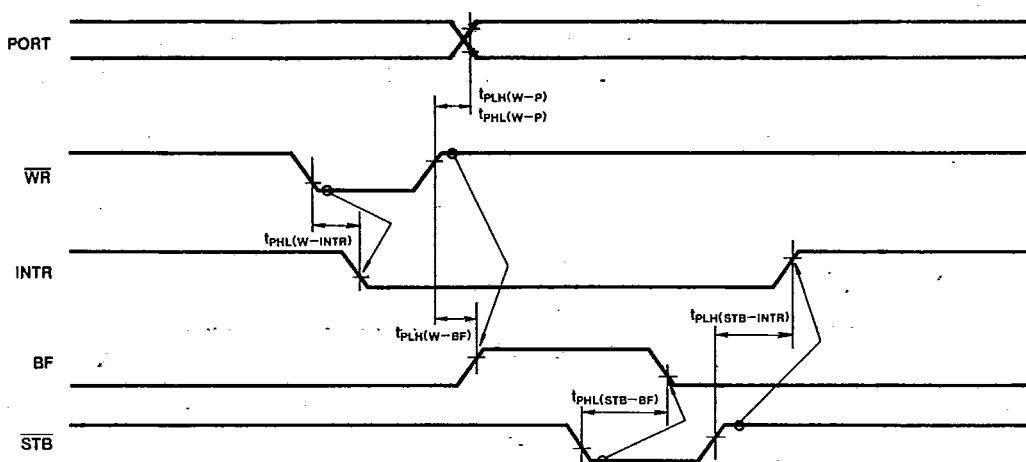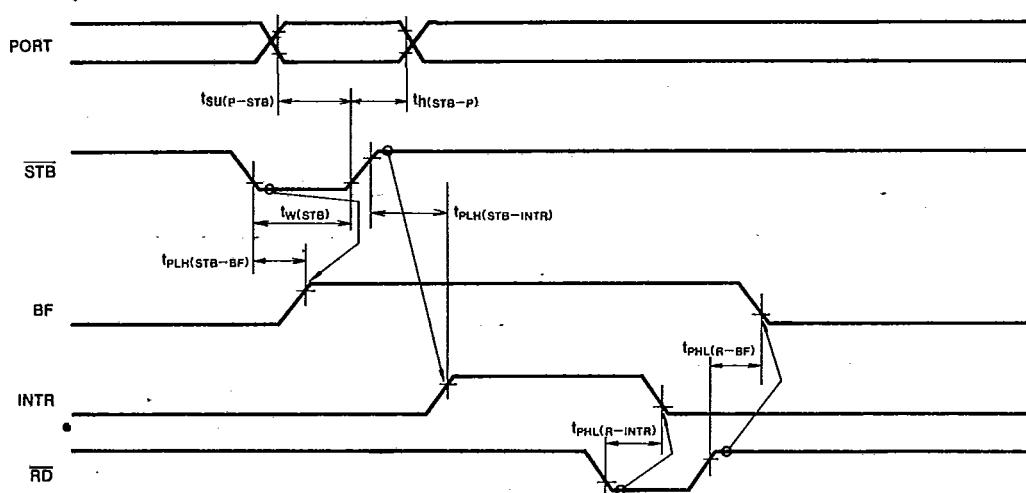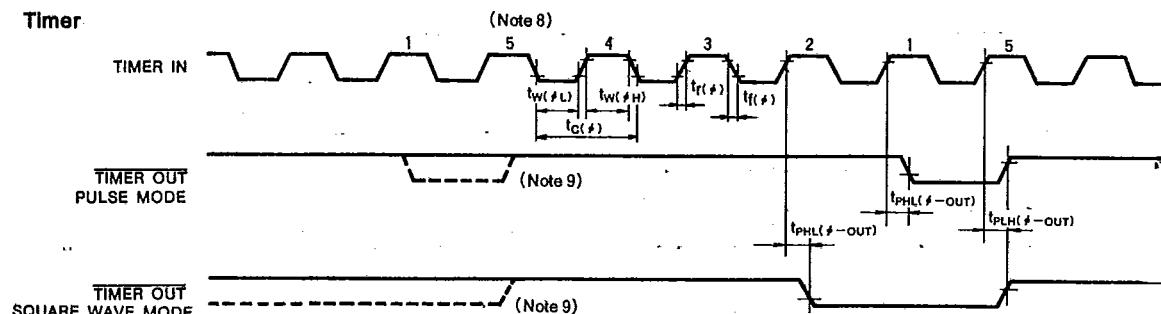
Note 8 : The wave form is shown for the case of counting down from 5 to 1.
     9 : As long as the M1 mode flag of the timer register is at
        high-level, pulses are continuously output.

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