

## Single-chip 8-bit microcontroller

8031AH/8051AH

## DESCRIPTION

The Philips 8031AH/8051AH is a high-performance microcontroller fabricated with Philips high-density highly reliable +5V, depletion-load, N-channel, silicon-gate, N500 MOS process technology. It provides the hardware features, architectural enhancements and instructions that are necessary to make it a powerful and cost-effective controller for applications requiring up to 64k bytes of program memory and/or up to 64k bytes of data storage.

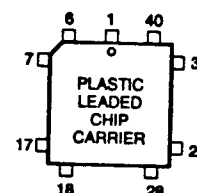
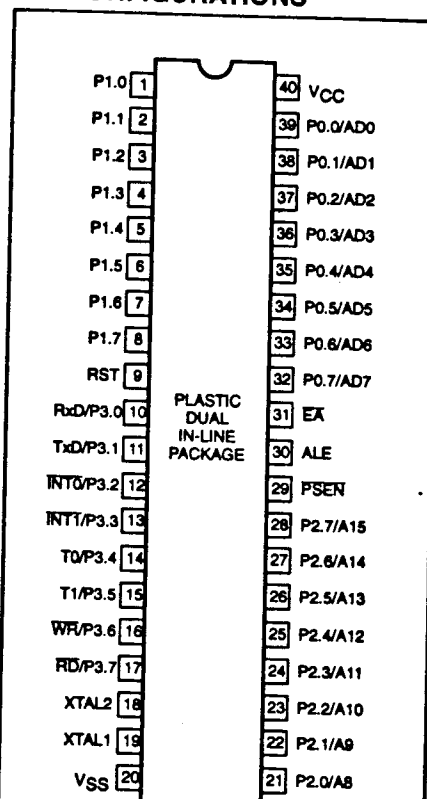
The 8051AH contains a 4k × 8 read-only program memory, a 128 × 8 read-only data memory, 32 I/O lines, two 16-bit counter/timers, a five-source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits. The 8031AH is identical, except that it lacks the program memory. For systems that require extra capability, the 8051AH can be expanded using standard TTL compatible memories and byte oriented peripheral controllers.

The 8051AH microcontroller, like its 8048 predecessor, is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12MHz crystal, 58% of the instructions execute in 1µs, 40% in 2µs and multiply and divide require only 4µs.

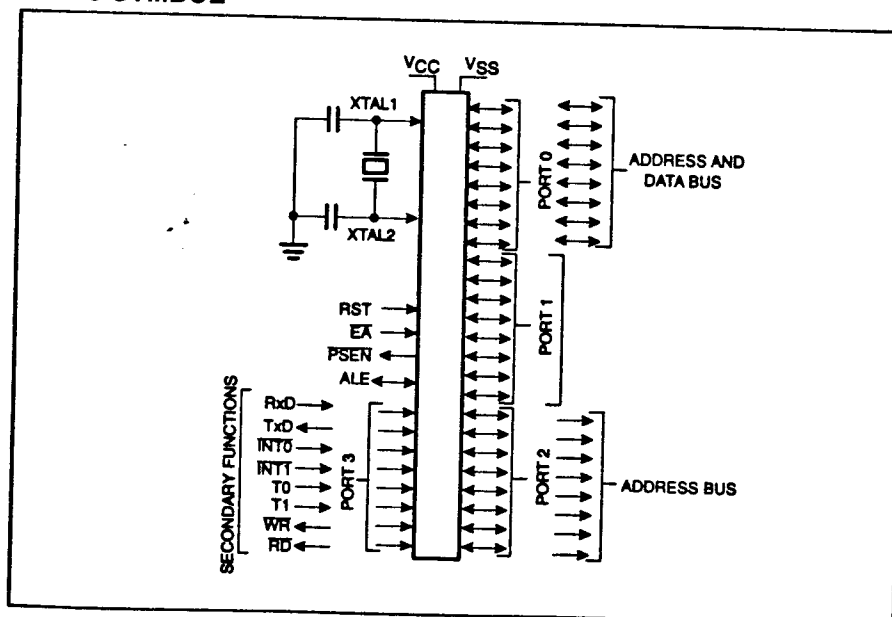
## FEATURES

- Reduced supply current
- 4k × 8 ROM (8051AH)
- 128 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- High-performance full-duplex serial channel
- External memory expandable to 128k
- Boolean processor
- Industry standard 8051 architecture:
  - Non-paged jumps
  - Direct addressing
  - Four 8-register banks
  - Stack depth up to 128-bytes
  - Multiply, divide, subtract, compare
- Most instructions execute in 1µs
- 4µs multiply and divide

## PIN CONFIGURATIONS



## LOGIC SYMBOL



| Pin | Function  | Pin | Function  | Pin | Function |
|-----|-----------|-----|-----------|-----|----------|
| 1   | NC        | 15  | INT1/P3.3 | 30  | P2.6/A14 |
| 2   | P1.0      | 16  | T0/P3.4   | 31  | P2.7/A15 |
| 3   | P1.1      | 17  | T1/P3.5   | 32  | PSEN     |
| 4   | P1.2      | 18  | WR/P3.6   | 33  | ALE      |
| 5   | P1.3      | 19  | RD/P3.7   | 34  | NC       |
| 6   | P1.4      | 20  | XTAL2     | 35  | EX       |
| 7   | P1.5      | 21  | XTAL1     | 36  | P0.7/AD7 |
| 8   | P1.6      | 22  | VSS       | 37  | P0.6/AD6 |
| 9   | P1.7      | 23  | NC        | 38  | P0.5/AD5 |
| 10  | RST       | 24  | P2.0/A8   | 39  | P0.4/AD4 |
| 11  | RxD/P3.0  | 25  | P2.1/A9   | 40  | P0.3/AD3 |
| 12  | NC        | 26  | P2.2/A10  | 41  | P0.2/AD2 |
| 13  | TxD/P3.1  | 27  | P2.3/A11  | 42  | P0.1/AD1 |
| 14  | INT0/P3.2 | 28  | P2.4/A12  | 43  | P0.0/AD0 |
|     |           | 29  | P2.5/A13  | 44  | VCC      |

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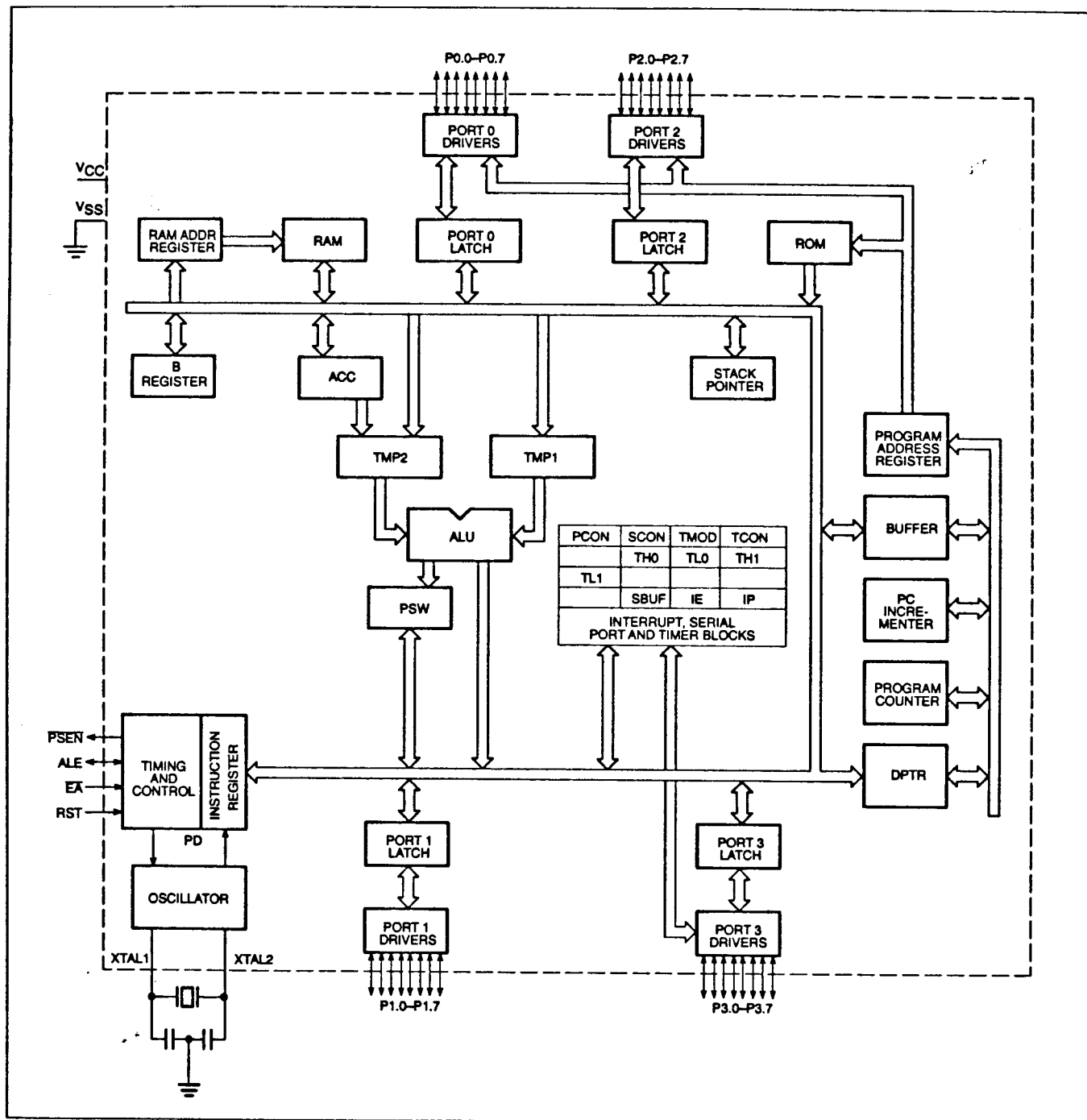
## PART NUMBER SELECTION

| PHILIPS                        |                              |               | PHILIPS NORTH AMERICA |               | TEMPERATURE<br>°C<br>AND PACKAGE               | FREQ.<br>MHz | DRAWING<br>NUMBER |
|--------------------------------|------------------------------|---------------|-----------------------|---------------|------------------------------------------------|--------------|-------------------|
| ROMless<br>(MARKING<br>NUMBER) | ROMless<br>(ORDER<br>NUMBER) | ROM           | ROMless               | ROM           |                                                |              |                   |
| MAF8031AH-2-12P                | MAF8031A-2 N                 | MAF8051AH-2P  | SCN8031HACN40         | SCN8051HACN40 | -40 to +85,<br>Plastic Dual<br>In-Line Package | 12           | 0415C             |
| MAB8031AH-2-12P                | MAB8031A-2 N                 | MAB8051AH-2P  | SCN8031HCCN40         | SCN8051HCCN40 | 0 to +70,<br>Plastic Dual<br>In-Line Package   | 12           | 0415C             |
|                                |                              |               | SCN8031HCFN40         | SCN8051HCFN40 | 0 to +70,<br>Plastic Dual<br>In-Line Package   | 15           | 0415C             |
|                                |                              |               | SCN8031HAFN40         | SCN8051HAFN40 | -40 to +85,<br>Plastic Dual<br>In-Line Package | 15           | 0415C             |
| MAB8031AH-2-12WP               | MAB8031A-2 A                 | MAB8051AH-2WP | SCN8031HCCA44         | SCN8051HCCA44 | 0 to +70,<br>Plastic Leaded<br>Chip Carrier    | 12           | 0403G             |
| MAF8031AH-2-12WP               | MAF8031A-2 A                 | MAF8051AH-2WP | SCN8031HACA44         | SCN8051HACA44 | -40 to +85,<br>Plastic Leaded<br>Chip Carrier  | 12           | 0403G             |
|                                |                              |               | SCN8031HCFA44         | SCN8051HCFA44 | 0 to +70,<br>Plastic Leaded<br>Chip Carrier    | 15           | 0403G             |
|                                |                              |               | SCN8031HAFA44         | SCN8051HAFA44 | -40 to +85,<br>Plastic Leaded<br>Chip Carrier  | 15           | 0403G             |

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### BLOCK DIAGRAM



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8031AH/8051AH

## PIN DESCRIPTIONS

| MNEMONIC        | PIN NO. |           | TYPE | NAME AND FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-----------------|---------|-----------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                 | DIP     | LCC       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| V <sub>SS</sub> | 20      | 22        | I    | Ground: 0V reference.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| V <sub>CC</sub> | 40      | 44        | I    | <b>Power Supply:</b> This is the power supply voltage for normal, idle, and power-down operation.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| P0.0–P0.7       | 39–32   | 43–36     | I/O  | <b>Port 0:</b> Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.                                                                                                                                                                                                                                                                                                                                                                                                                |
| P1.0–P1.7       | 1–8     | 2–9       | I/O  | <b>Port 1:</b> Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I <sub>IL</sub> ).                                                                                                                                                                                                                                                                                                                                                                                                   |
| P2.0–P2.7       | 21–28   | 24–31     | I/O  | <b>Port 2:</b> Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I <sub>IL</sub> ). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register. |
| P3.0–P3.7       | 10–17   | 11, 13–19 | I/O  | <b>Port 3:</b> Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I <sub>IL</sub> ). Port 3 also serves the special features of the 80C51 family, as listed below:                                                                                                                                                                                                                                                                                                                        |
|                 | 10      | 11        | I    | RxD (P3.0): Serial input port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|                 | 11      | 13        | O    | TxD (P3.1): Serial output port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|                 | 12      | 14        | I    | INT0 (P3.2): External interrupt                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|                 | 13      | 15        | I    | INT1 (P3.3): External interrupt                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|                 | 14      | 16        | I    | T0 (P3.4): Timer 0 external input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|                 | 15      | 17        | I    | T1 (P3.5): Timer 1 external input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|                 | 16      | 18        | O    | WR (P3.6): External data memory write strobe                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|                 | 17      | 19        | O    | RD (P3.7): External data memory read strobe                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| RST             | 9       | 10        | I    | <b>Reset:</b> A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V <sub>SS</sub> permits a power-on reset using only an external capacitor to V <sub>CC</sub> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| ALE             | 30      | 33        | I/O  | <b>Address Latch Enable:</b> Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory.                                                                                                                                                                                                                                                                                                                                                                                                                    |
| PSEN            | 29      | 32        | O    | <b>Program Store Enable:</b> The read strobe to external program memory. When the device is executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.                                                                                                                                                                                                                                                                                                                                                                                                               |
| EA              | 31      | 35        | I    | <b>External Access Enable:</b> EA must be externally held low to enable the device to fetch code from external program memory locations 0000H to 0FFFH. If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 0FFFH.                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| XTAL1           | 19      | 21        | I    | <b>Crystal 1:</b> Input to the inverting oscillator amplifier.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| XTAL2           | 18      | 20        | O    | <b>Crystal 2:</b> Output from the inverting oscillator amplifier and input to the internal clock generator circuits.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

## OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol.

To drive the device from an external clock source, XTAL2 should be driven while XTAL1 is connected to ground. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum

high and low times specified in the data sheet must be observed.

## DESIGN CONSIDERATIONS

At power-on, the voltage on V<sub>CC</sub> and RST should come up at the same time for a proper start-up.

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8031AH/8051AH

ABSOLUTE MAXIMUM RATINGS<sup>1, 2, 3</sup>

| PARAMETER                               | RATING       | UNIT |
|-----------------------------------------|--------------|------|
| Storage temperature range               | -65 to +150  | °C   |
| Voltage on any other pin to $V_{SS}$    | -0.5 to +7.0 | V    |
| Input, output current on any single pin | 10           | mA   |
| Power dissipation                       | 1.0          | W    |

## DC ELECTRICAL CHARACTERISTICS

 $T_{amb} = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$ <sup>4, 5</sup>

| SYMBOL    | PARAMETER                                           | TEST CONDITIONS                            | LIMITS |              | UNIT          |
|-----------|-----------------------------------------------------|--------------------------------------------|--------|--------------|---------------|
|           |                                                     |                                            | MIN    | MAX          |               |
| $V_{IL}$  | Input low voltage                                   |                                            | -0.5   | 0.8          | V             |
| $V_{IH}$  | Input high voltage; except XTAL2, RST               |                                            | 2.0    | $V_{CC}+0.5$ | V             |
| $V_{IH1}$ | Input high voltage to RST for reset, XTAL2          | XTAL1 to $V_{SS}$                          | 2.5    | $V_{CC}+0.5$ | V             |
| $V_{OL}$  | Output low voltage; ports 1, 2, 3 <sup>6</sup>      | $I_{OL} = 1.6\text{mA}$                    |        | 0.45         | V             |
| $V_{OL1}$ | Output low voltage; port 0, ALE, PSEN <sup>6</sup>  | $I_{OL} = 3.2\text{mA}$                    |        | 0.45         | V             |
| $V_{OH}$  | Output high voltage; ports 1, 2, 3                  | $I_{OH} = -80\mu\text{A}$                  | 2.4    |              | V             |
| $V_{OH1}$ | Output high voltage; port 0, ALE, PSEN <sup>3</sup> | $I_{OH} = -400\mu\text{A}$                 | 2.4    |              | V             |
| $I_{IL}$  | Logical 0 input current; ports 1, 2, 3              | $V_{IN} = 0.45\text{V}$                    |        | -500         | $\mu\text{A}$ |
| $I_{IH1}$ | Input high current to RST for reset                 | $V_{IN} < V_{CC} - 1.5\text{V}$            |        | 500          | $\mu\text{A}$ |
| $I_{LI}$  | Input leakage current; port 0, EA                   | $0.45 < V_{IN} < V_{CC}$                   |        | $\pm 10$     | $\mu\text{A}$ |
| $I_{IL2}$ | Logical 0 input current for XTAL2                   | XTAL1 = $V_{SS}$ , $V_{IN} = 0.45\text{V}$ |        | -3.2         | mA            |
| $I_{CC}$  | Power supply current                                | All outputs disconnected and EA = $V_{CC}$ |        | 125          | mA            |
| $C_{IO}$  | Pin capacitance                                     |                                            |        | 10           | pF            |

 $T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$ 

| SYMBOL    | PARAMETER                             | TEST CONDITIONS                            | LIMITS |              | UNIT |
|-----------|---------------------------------------|--------------------------------------------|--------|--------------|------|
|           |                                       |                                            | MIN    | MAX          |      |
| $V_{IH}$  | Input high voltage; except XTAL2, RST |                                            | 2.1    | $V_{CC}+0.5$ | V    |
| $V_{IH1}$ | Input high voltage to RST and XTAL2   | XTAL1 = $V_{SS}$                           | 2.6    | $V_{CC}+0.5$ | V    |
| $I_{IL2}$ | Logical 0 input current for XTAL2     | XTAL1 = $V_{SS}$ , $V_{IN} = 0.45\text{V}$ |        | -4.0         | mA   |
| $I_{CC}$  | Power supply current                  | All outputs disconnected and EA = $V_{CC}$ |        | 135          | mA   |

## NOTES:

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
- For operating at elevated temperatures, the device must be derated based on  $+150^{\circ}\text{C}$  maximum junction temperature.
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
- Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to  $V_{SS}$  unless otherwise noted.
- All voltage measurements are referenced to ground. For testing, all input signals swing between 0.45V and 2.4V with a transition time of 20ns maximum. All time measurements are referenced at input voltages of 0.8V and 2.0V and at output voltages of 0.8V and 2.0V as appropriate.
- $V_{OL}$  is derated when the device rapidly discharges external capacitance. This AC noise is most pronounced during emission of address data. When using external memory, locate the latch or buffer as close as possible to the device.

| Datum      | Emitting Ports | Degraded I/O Lines | $V_{OL}$ (Peak Max) |
|------------|----------------|--------------------|---------------------|
| Address    | P2, P0         | P1, P3             | 0.8V                |
| Write Data | P0             | P1, p3, ALE        | 0.8V                |

- $C_L = 100\text{pF}$  for port 0, ALE and PSEN outputs;  $C_L = 80\text{pF}$  for all other ports.

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8031AH/8051AH

## AC ELECTRICAL CHARACTERISTICS

 $T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C or } -40^{\circ}\text{C to } +85^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V} \pm 20\%$ ,  $V_{SS} = 0\text{V}^{1,2}$ 

| SYMBOL         | FIGURE | PARAMETER                                                                                              | 12MHz CLOCK |     | VARIABLE CLOCK           |                      | UNIT                     |
|----------------|--------|--------------------------------------------------------------------------------------------------------|-------------|-----|--------------------------|----------------------|--------------------------|
|                |        |                                                                                                        | MIN         | MAX | MIN                      | MAX                  |                          |
| $1/t_{CLCL}$   |        | Oscillator frequency: Speed Versions<br>SCN8051/31 C<br>MAB8051/31 -2<br>MAF8051/31 -2<br>SCN8051/31 F |             |     | 3.5<br>3.5<br>3.5<br>3.5 | 12<br>12<br>12<br>15 | MHz<br>MHz<br>MHz<br>MHz |
| $t_{LHL}$      | 1      | ALE pulse width                                                                                        | 127         |     | $2t_{CLCL}-40$           |                      | ns                       |
| $t_{AVLL}$     | 1      | Address valid to ALE low                                                                               | 43          |     | $t_{CLCL}-40$            |                      | ns                       |
| $t_{LLAX}$     | 1      | Address hold after ALE low                                                                             | 48          |     | $t_{CLCL}-35$            |                      | ns                       |
| $t_{LLIV}$     | 1      | ALE low to valid instruction in                                                                        |             | 233 |                          | $4t_{CLCL}-100$      | ns                       |
| $t_{LLPL}$     | 1      | ALE low to PSEN low                                                                                    | 58          |     | $t_{CLCL}-25$            |                      | ns                       |
| $t_{PLPH}$     | 1      | PSEN pulse width                                                                                       | 215         |     | $3t_{CLCL}-35$           |                      | ns                       |
| $t_{PLIV}$     | 1      | PSEN low to valid instruction in                                                                       |             | 125 |                          | $3t_{CLCL}-125$      | ns                       |
| $t_{PXIX}$     | 1      | Input instruction hold after PSEN                                                                      | 0           |     | 0                        |                      | ns                       |
| $t_{PXIZ}$     | 1      | Input instruction float after PSEN                                                                     |             | 63  |                          | $t_{CLCL}-20$        | ns                       |
| $t_{AVIV}$     | 1      | Address to valid instruction in                                                                        |             | 302 |                          | $5t_{CLCL}-115$      | ns                       |
| $t_{PLAZ}$     | 1      | PSEN low to address float                                                                              |             | 20  |                          | 20                   | ns                       |
| $t_{PXAV}$     | 1      | PSEN to address valid                                                                                  | 75          |     | $t_{CLCL}-8$             |                      | ns                       |
| Data Memory    |        |                                                                                                        |             |     |                          |                      |                          |
| $t_{RLRH}$     | 2, 3   | RD pulse width                                                                                         | 400         |     | $6t_{CLCL}-100$          |                      | ns                       |
| $t_{WLWH}$     | 2, 3   | WR pulse width                                                                                         | 400         |     | $6t_{CLCL}-100$          |                      | ns                       |
| $t_{RLDV}$     | 2, 3   | RD low to valid data in                                                                                |             | 252 |                          | $5t_{CLCL}-165$      | ns                       |
| $t_{RHDX}$     | 2, 3   | Data hold after RD                                                                                     | 0           |     | 0                        |                      | ns                       |
| $t_{RHDZ}$     | 2, 3   | Data float after RD                                                                                    |             | 97  |                          | $2t_{CLCL}-70$       | ns                       |
| $t_{LLDV}$     | 2, 3   | ALE low to valid data in                                                                               |             | 517 |                          | $8t_{CLCL}-150$      | ns                       |
| $t_{AVDV}$     | 2, 3   | Address to valid data in                                                                               |             | 585 |                          | $9t_{CLCL}-165$      | ns                       |
| $t_{LLWL}$     | 2, 3   | ALE low to RD or WR low                                                                                | 200         | 300 | $3t_{CLCL}-50$           | $3t_{CLCL}+50$       | ns                       |
| $t_{AVWL}$     | 2, 3   | Address valid to WR low or RD low                                                                      | 203         |     | $4t_{CLCL}-130$          |                      | ns                       |
| $t_{QVWX}$     | 2, 3   | Data valid to WR transition                                                                            | 23          |     | $t_{CLCL}-60$            |                      | ns                       |
| $t_{QVWH}$     | 2, 3   | Data valid to WR high                                                                                  | 433         |     | $7t_{CLCL}-150$          |                      | ns                       |
| $t_{WHQX}$     | 2, 3   | Data hold after WR                                                                                     | 33          |     | $t_{CLCL}-50$            |                      | ns                       |
| $t_{RLAZ}$     | 2, 3   | RD low to address float                                                                                |             | 20  |                          | 20                   | ns                       |
| $t_{WHLH}$     | 2, 3   | RD or WR high to ALE high                                                                              | 43          | 123 | $t_{CLCL}-40$            | $t_{CLCL}+40$        | ns                       |
| External Clock |        |                                                                                                        |             |     |                          |                      |                          |
| $t_{CHCX}$     | 5      | High time                                                                                              | 20          |     | 20                       |                      | ns                       |
| $t_{CLCX}$     | 5      | Low time                                                                                               | 20          |     | 20                       |                      | ns                       |
| $t_{CLCH}$     | 5      | Rise time                                                                                              |             | 20  |                          | 20                   | ns                       |
| $t_{CHCL}$     | 5      | Fall time                                                                                              |             | 20  |                          | 20                   | ns                       |

## NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.

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8031AH/8051AH

## EXPLANATION OF THE AC SYMBOLS

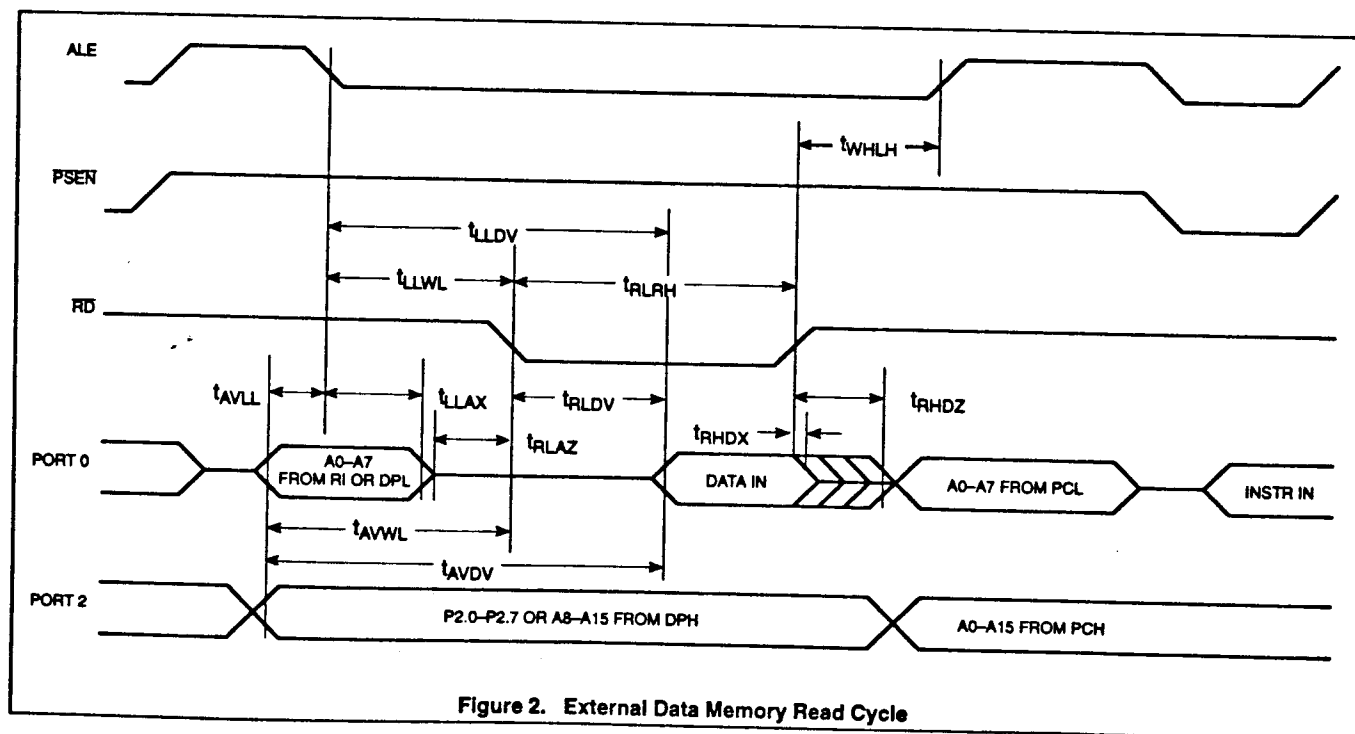
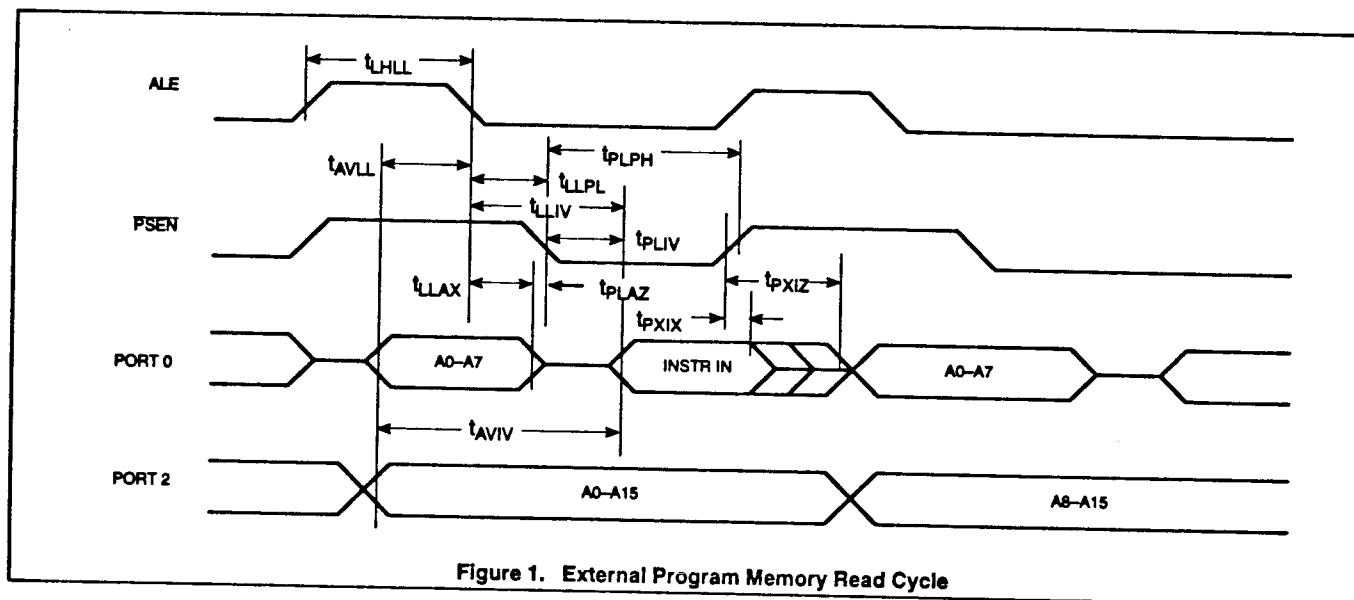
Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A - Address  
C - Clock  
D - Input data  
H - Logic level high  
I - Instruction (program memory contents)  
L - Logic level low, or ALE  
P - PSEN

Q - Output data  
R - RD signal  
t - Time  
V - Valid  
W - WR signal  
X - No longer a valid logic level  
Z - Float

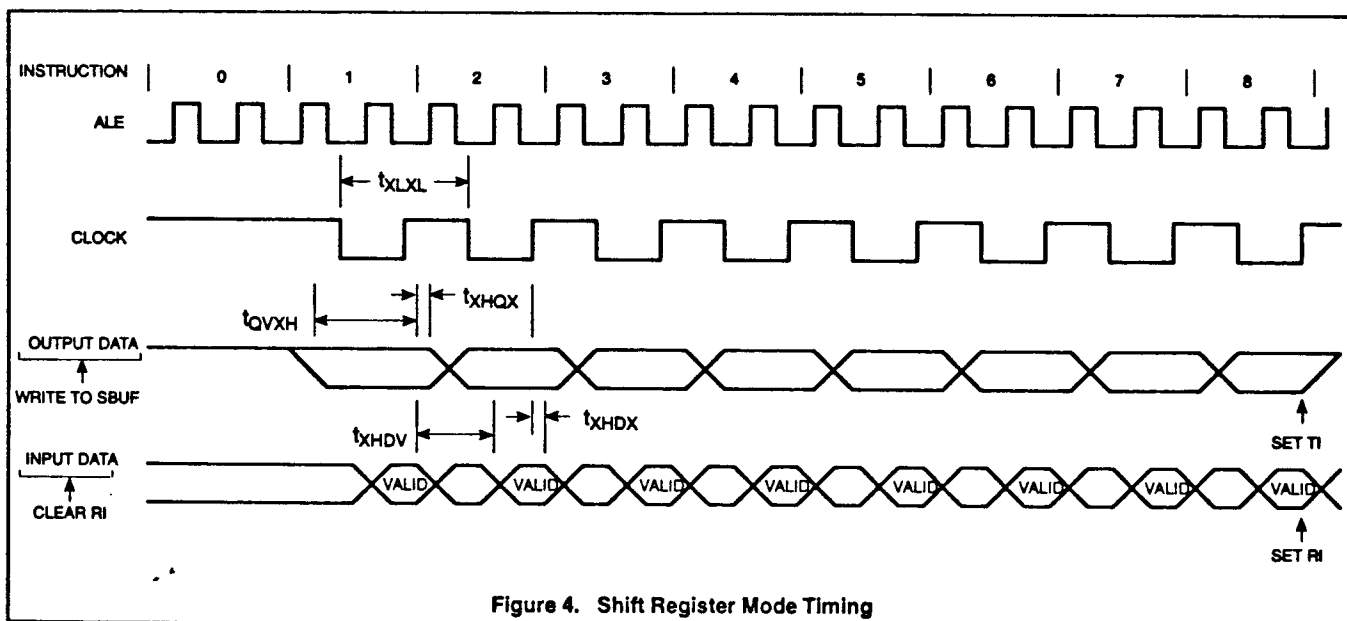
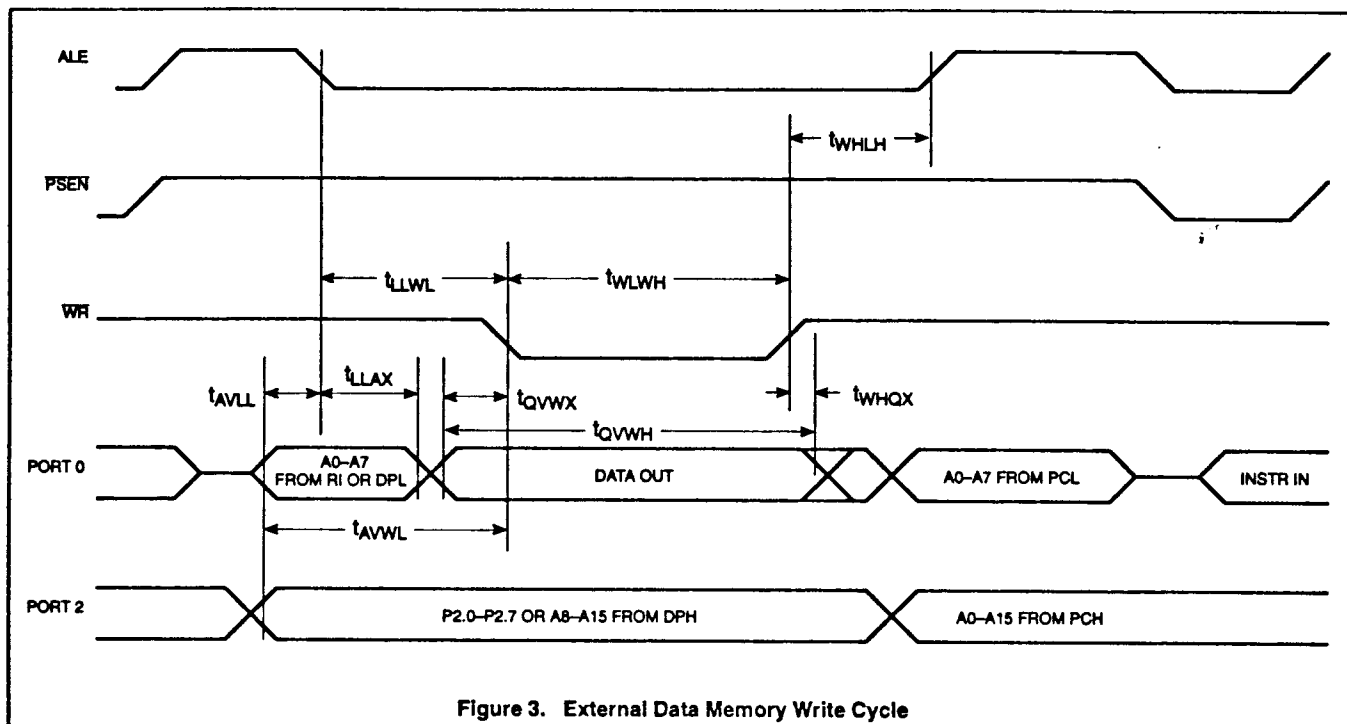
Examples:  $t_{AVLL}$  = Time for address valid to ALE low.

$t_{LLPL}$  = Time for ALE low to PSEN low.



## Single-chip 8-bit microcontroller

8031AH/8051AH





## Single-chip 8-bit microcontroller

8031AH/8051AH

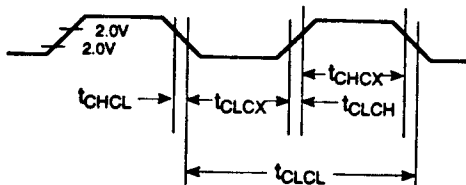
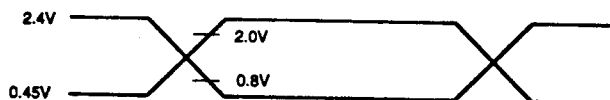
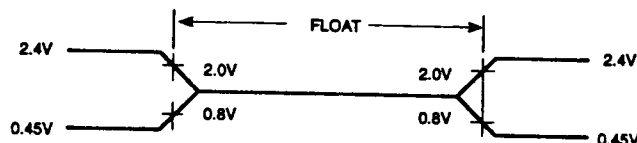


Figure 5. External Clock Drive



NOTE:  
AC inputs during testing are driven at 2.4V for a logic '1' and 0.45V for a logic '0'.  
Timing measurements are made at 2.0V min for a logic '1' and 0.8V for a logic '0'.

Figure 6. AC Testing Input/Output



NOTE:  
For timing purposes, the float state is defined as the point at which a P0 pin sinks 2.4mA or sources 400μA at the voltage test levels.

Figure 7. Float Waveform

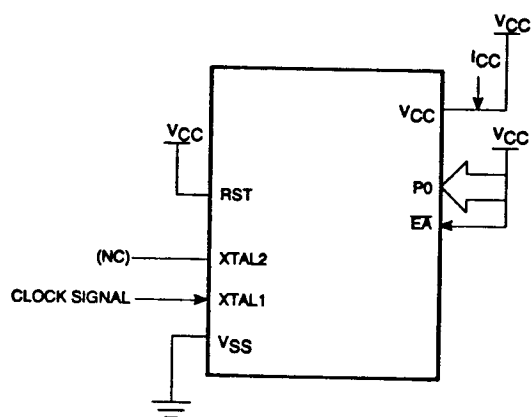


Figure 8.  $I_{CC}$  Test Condition, Active Mode  
All other pins are disconnected

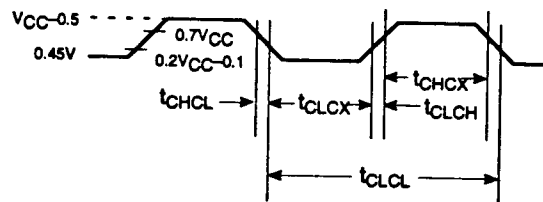


Figure 9. Clock Signal Waveform for  
 $I_{CC}$  Tests in Active and Idle Modes  
 $t_{CLCH} = t_{CHCL} = 5\text{ns}$