

30A, 50V, 0.065 Ohm, P-Channel Power MOSFETs

These are P-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA09834.

Ordering Information

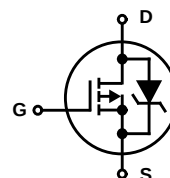
PART NUMBER	PACKAGE	BRAND
RFG30P05	TO-247	RFG30P05
RFP30P05	TO-220AB	RFP30P05
RF1S30P05SM	TO-263AB	F1S30P05

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, i.e., RF1S30P05SM9A.

Features

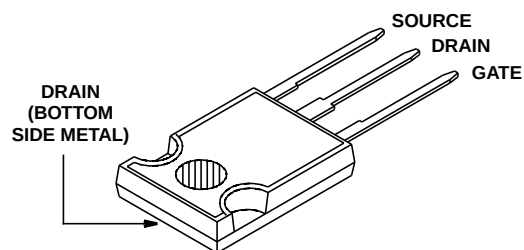
- 30A, 50V
- $r_{DS(ON)} = 0.065\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

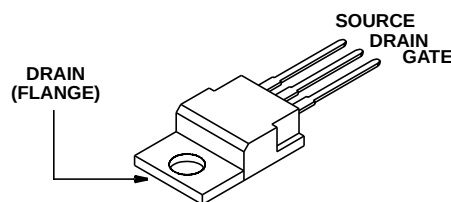


Packaging

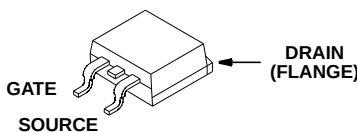
JEDEC STYLE TO-247



JEDEC TO-220AB



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

	RFG30P05, RFP30P05 RF1S30P05SM	UNITS
Drain to Source Voltage (Note 1)	V_{DSS} -50	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR} -50	V
Gate to Source Voltage	V_{GS} ± 20	V
Continuous Drain Current	I_D 30	A
Pulsed Drain Current (Note 3) (Figure 5)	I_{DM} Refer to Peak Current Curve	
Power Dissipation	P_D 120	W
Linear Derating Factor	0.8	W/ $^{\circ}\text{C}$
Single Pulse Avalanche Rating (Figure 6)	E_{AS} Refer to UIS Curve	
Operating and Storage Temperature	T_J, T_{STG} -55 to 175	$^{\circ}\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L 300	$^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg} 260	$^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V		-50	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA		-2	-	-4	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Rated BV _{DSS} , V _{GS} = 0V		-	-	-1	μA
		V _{DS} = 0.8 x Rated BV _{DSS} , T _C = 150°C		-	-	-25	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V		-	-	±100	nA
Drain to Source On Resistance	r _{DS(ON)}	I _D = 30A, V _{GS} = -10V (Figure 9)		-	-	0.065	Ω
Turn-On Time	t _(ON)	V _{DD} = -25V, I _D = 15A, R _L = 1.67Ω, V _{GS} = -10V, R _G = 6.25Ω (Figure 13)		-	-	80	ns
Turn-On Delay Time	t _{d(ON)}			-	15	-	ns
Rise Time	t _r			-	23	-	ns
Turn-Off Delay Time	t _{d(OFF)}			-	28	-	ns
Fall Time	t _f			-	18	-	ns
Turn-Off Time	t _(OFF)			-	-	100	ns
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0 to -20V	V _{DD} = -40V, I _D = 30A, R _L = 1.33Ω, I _{G(REF)} = 1.6mA	-	140	170	nC
Gate Charge at -10V	Q _{g(-10)}	V _{GS} = 0 to -10V		-	70	85	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0 to -2V		-	5.5	6.6	nC
Input Capacitance	C _{ISS}	V _{DS} = -25V, V _{GS} = 0V f = 1MHz (Figure 12)		-	3200	-	pF
Output Capacitance	C _{OSS}			-	800	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	175	-	pF
Thermal Resistance, Junction to Case	R _{θJC}			-	-	1.25	°C/W
Thermal Resistance, Junction to Ambient	R _{θJA}	TO-220, TO-263		-	-	62	°C/W
		TO-247		-	-	30	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	$I_{SD} = -30\text{A}$	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	$I_{SD} = -30\text{A}$, $dI_{SD}/dt = -100\text{A}/\mu\text{s}$	-	-	150	ns

NOTES:

2. Pulsed: pulse duration = $300\mu\text{s}$ max, duty cycle = 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).

Typical Performance Curves Unless Otherwise Specified

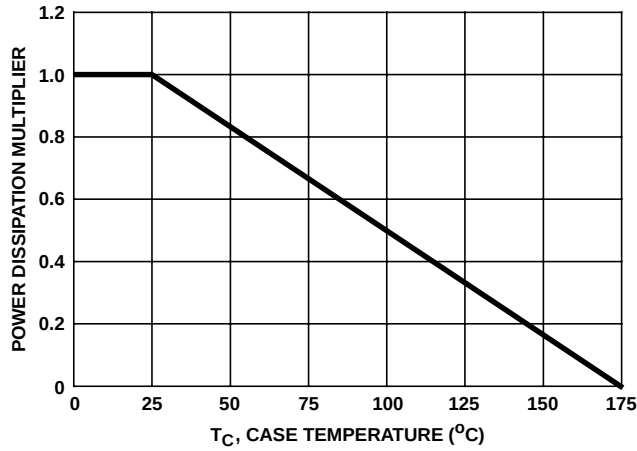


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

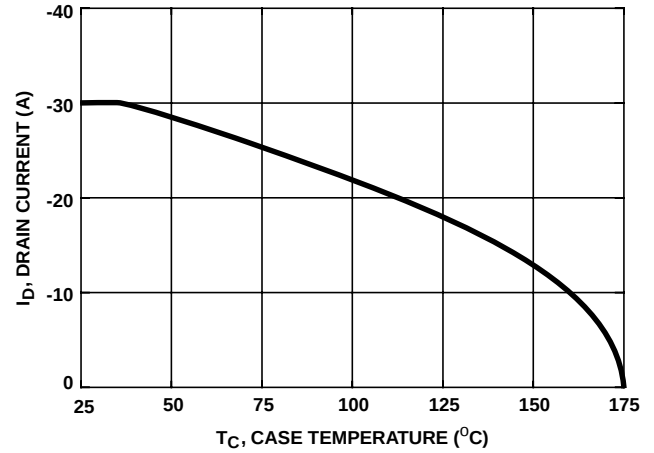


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

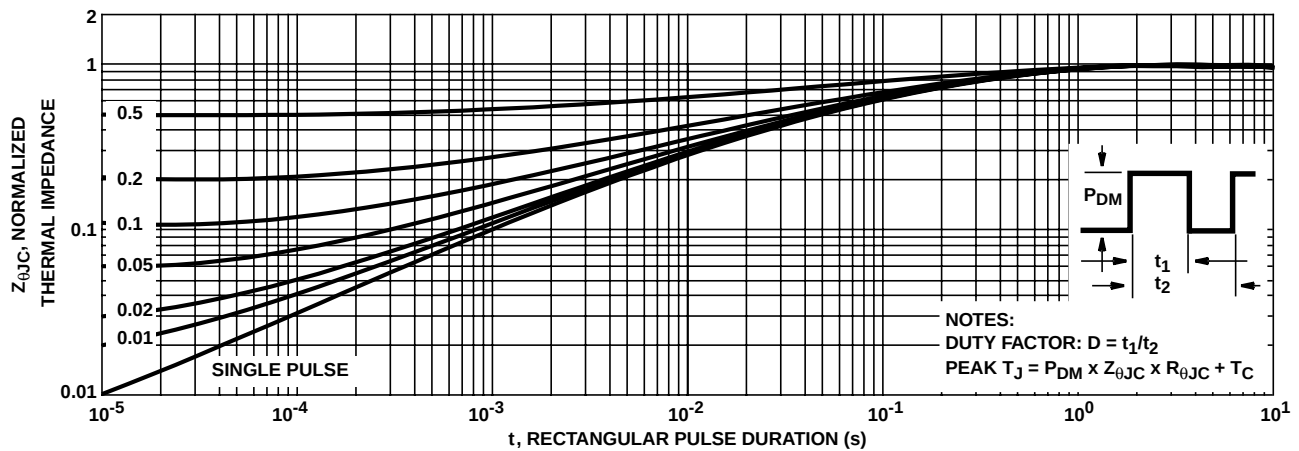


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

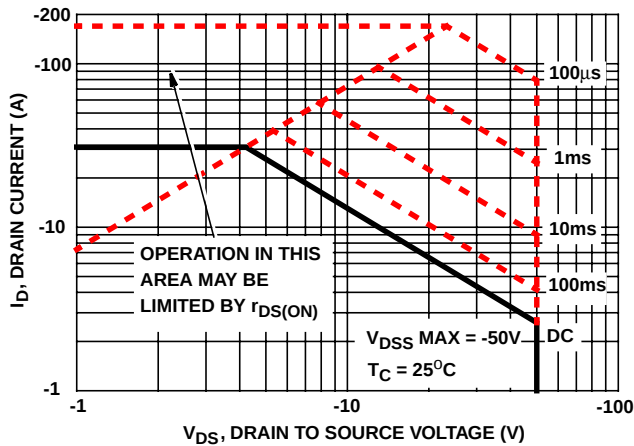


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

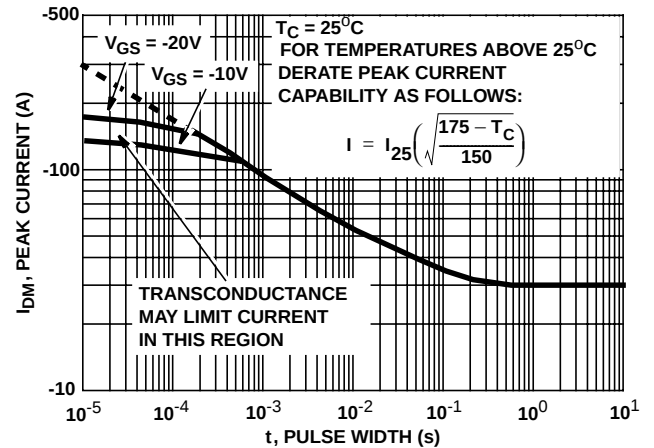
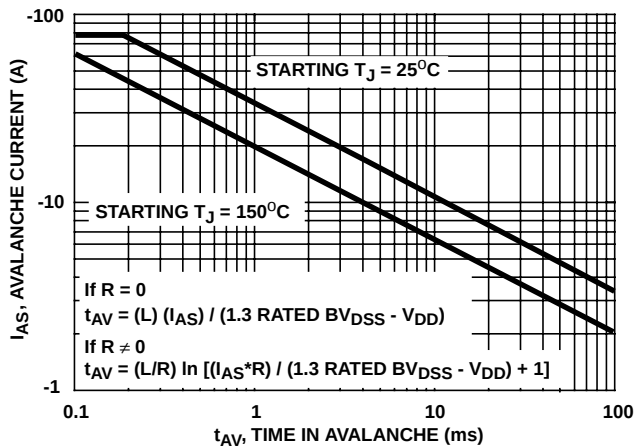


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

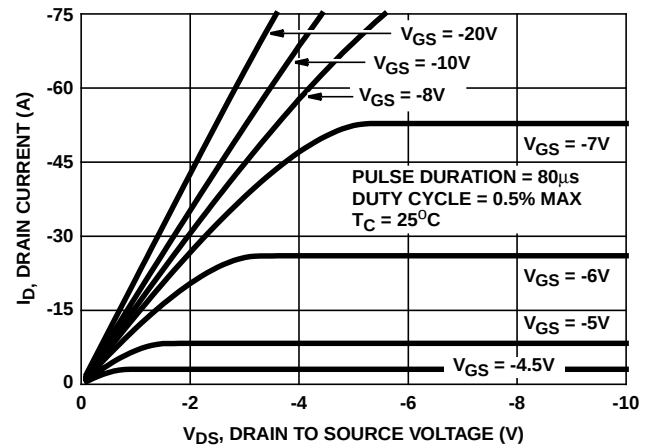


FIGURE 7. SATURATION CHARACTERISTICS

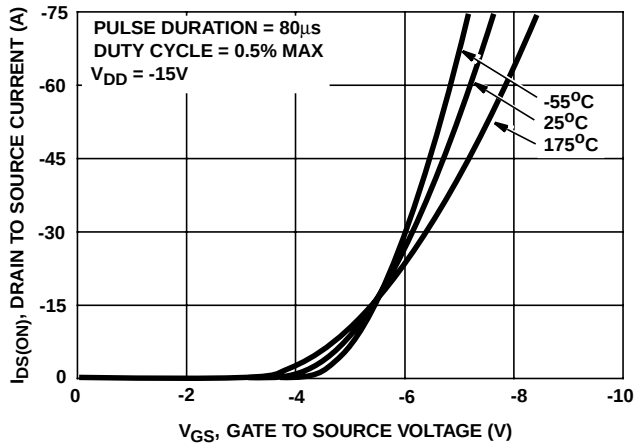


FIGURE 8. TRANSFER CHARACTERISTICS

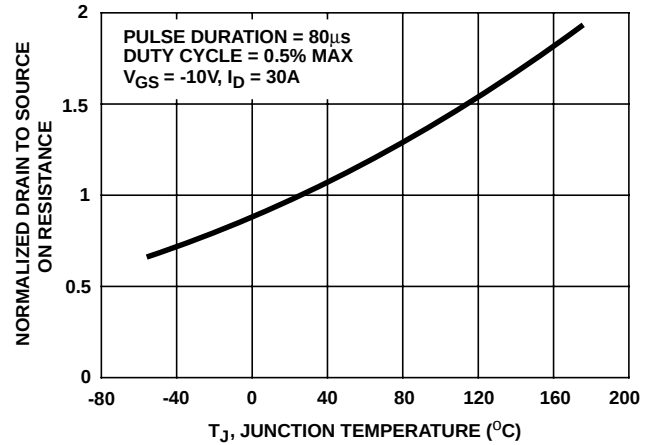


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

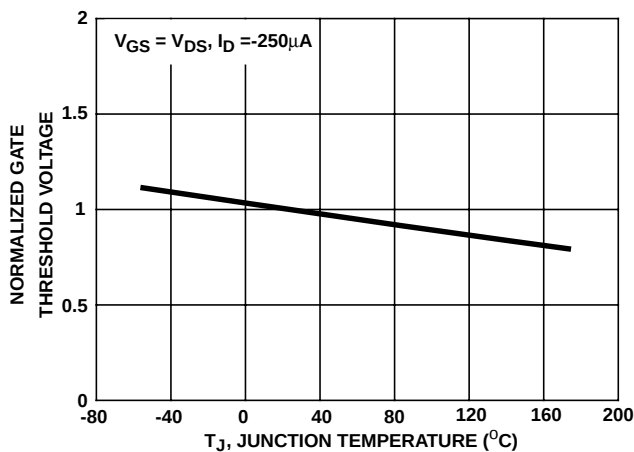


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

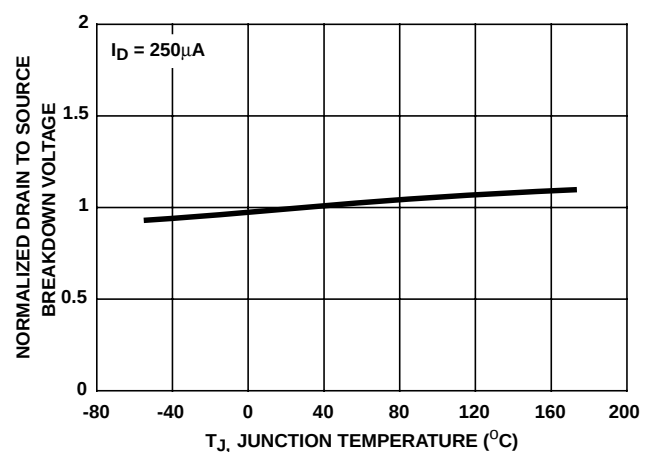


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

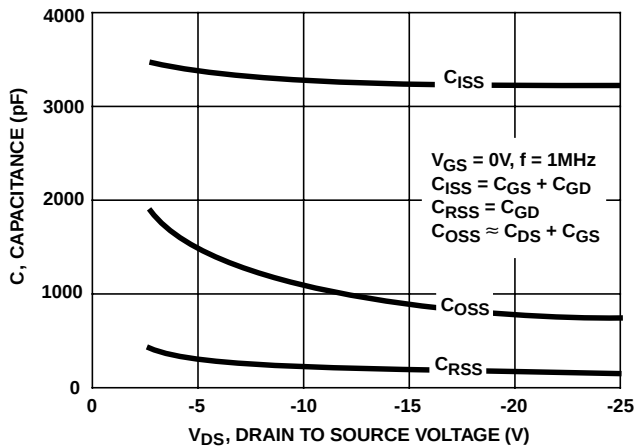
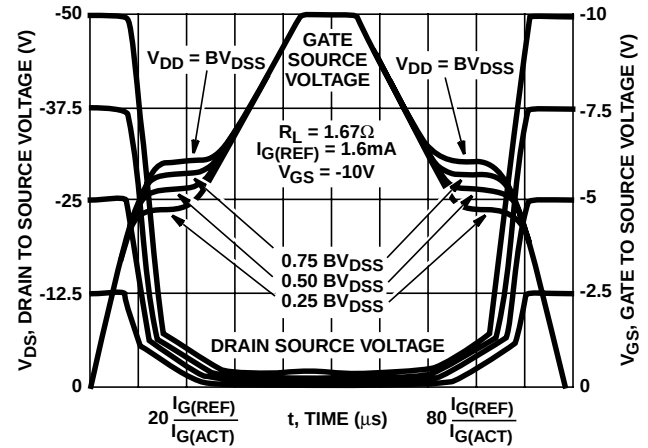


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

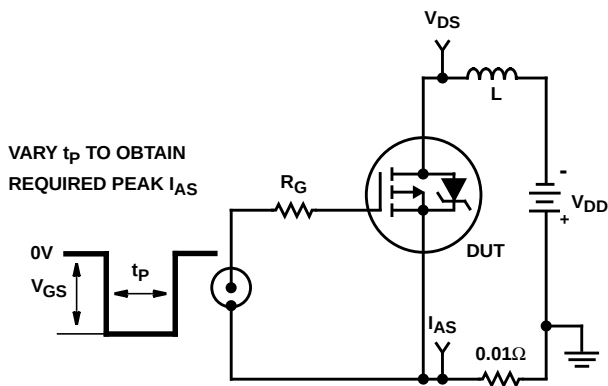


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

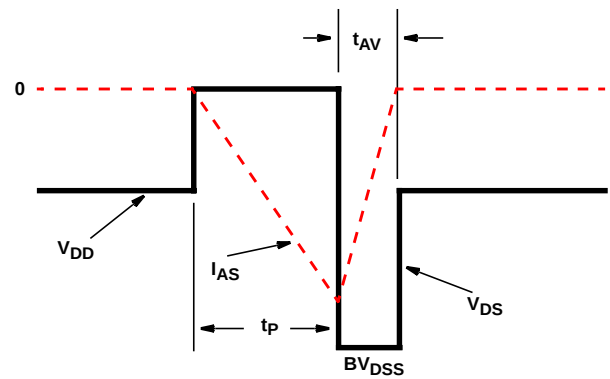


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

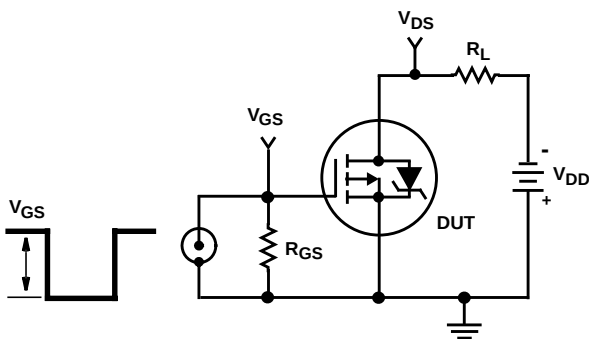


FIGURE 16. SWITCHING TIME TEST CIRCUIT

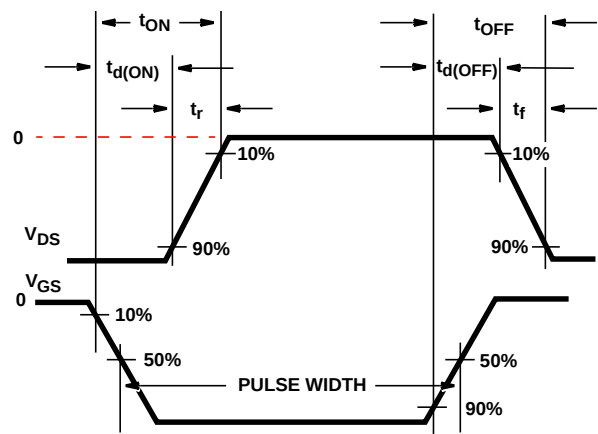


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

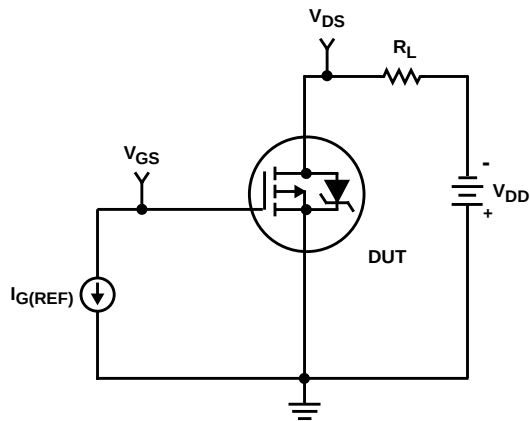


FIGURE 18. GATE CHARGE TEST CIRCUIT

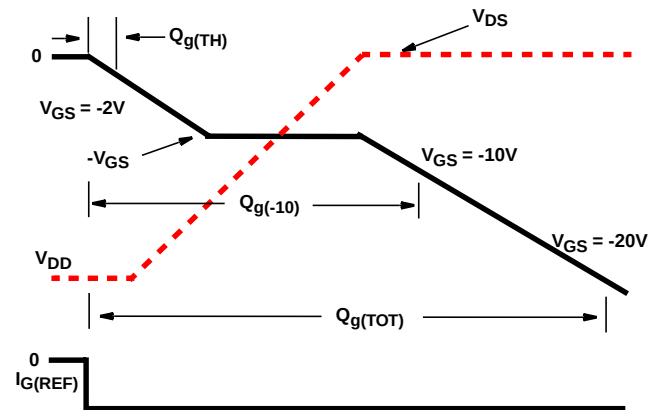


FIGURE 19. GATE CHARGE WAVEFORMS

PSPICE Electrical Model

.SUBCKT RFP30P05 2 1 3;
REV 8/21/94

CA 12 8 3.23e-9
CB 15 14 3.23e-9
CIN 6 8 3.08e-9

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -77.3
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 4.92e-9
LSOURCE 3 7 4.60e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 39.85e-3
RGATE 9 20 2.34
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 2.56e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

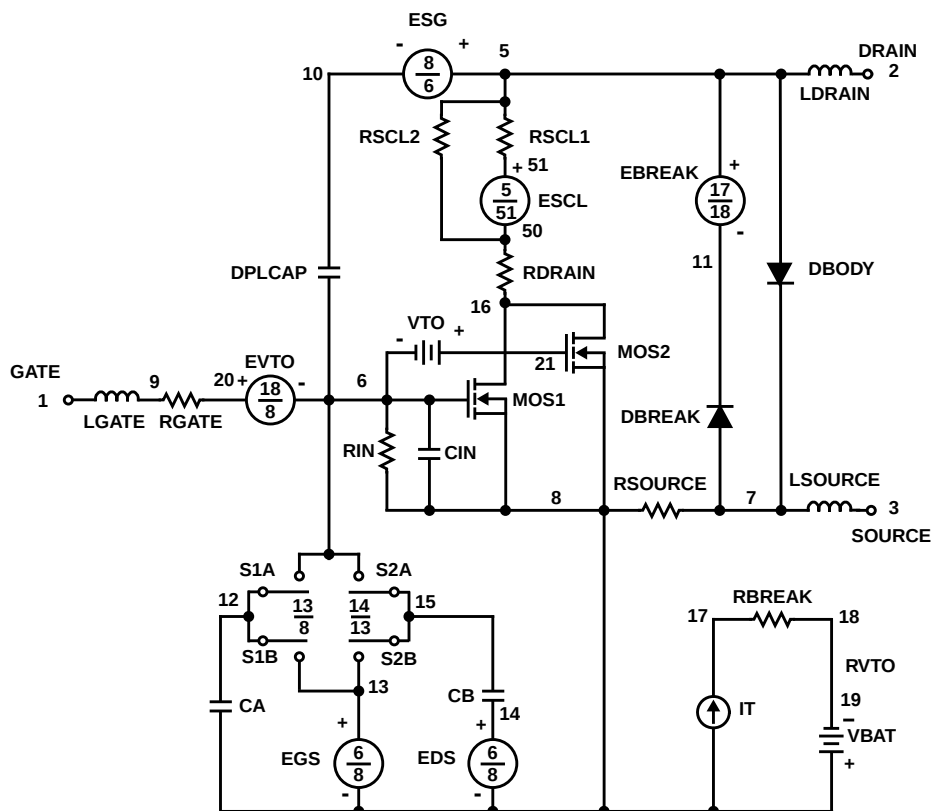
VBAT 8 19 DC 1
VTO 21 6 -0.81

ESCL 51 50 VALUE={ (V(5,51)/ABS(V(5,51))) * (PWR(V(5,51)*1e6/114,5)) }

.MODEL DBDMOD D (IS=4.7e-13 RS=1.31e-2 TRS1=1.39e-4 TRS2=-4.77e-6 CJO=2.85e-9 TT=8.81e-8)
.MODEL DBKMOD D (RS=2.23e-1 TRS1=1.97e-3 TRS2=-2.37e-5)
.MODEL DPLCAPMOD D (CJO=0.78e-9 IS=1e-30 N=10)
.MODEL MOSMOD PMOS (VTO=-3.75 KP=10.83 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=9.08e-4 TC2=-1.72e-6)
.MODEL RDSMOD RES (TC1=5.01e-3 TC2=1.02e-5)
.MODEL RSCLMOD RES (TC1=2.09e-3 TC2=5.88e-7)
.MODEL RVTOMOD RES (TC1=-2.99e-3 TC2=1.40e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=3.4 VOFF=1.4)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.4 VOFF=3.4)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.2 VOFF=-3.8)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.8 VOFF=1.2)

.ENDS

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; authors, William J. Hepp and C. Frank Wheatley.



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusée
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029