DL 257 D

4 Multiplexer 2 to 1, Tristate Outputs

Pin Assignment (DIP-16)

Pin	Function
1	S (Select input)
2	A1 (Data input A1)
3	B1 (Data input B1)
4	Y1 (Output 1)
5	A2 (Data input A2)
6	B2 (Data input B2)
7	Y2 (Output 2)
8	GND (Ground)
9	Y3 (Output 3)
10	B3 (Data input B3)
11	A3 (Data input A3)
12	Y4 (Output 4)
13	B4 (Data input B4)
14	A4 (Data input A4)
15	OE (Output Enable, active Low)
16	VCC (Supply voltage)

Functional Description

The DL 257 D contains four independent 2-to-1 multiplexers with tristate outputs.
Each multiplexer selects between two data inputs (A and B) based on the common select input S.

The outputs Y1-Y4 are enabled when OE (Output Enable) is Low.
When OE is High, all outputs are in high-impedance state (Z).

Select logic:
- S = Low: Output Y = A (data input A selected)
- S = High: Output Y = B (data input B selected)

Function Table

A	B	S	OE	Y
X	X	X	H	Z
L	X	L	L	L (A)
H	X	L	L	H (A)
X	L	H	L	L (B)
X	H	H	L	H (B)

X = Level arbitrary (L or H); Z = High impedance (Tristate)

Package Information

Package DL 257 D: DIP-16, Plastic (Figure 4)

Package DL 257 S: SO-16 (Figure 29)

Type standard: TGL 43295

Selected Parameters

Test conditions: CL = 50 pF; RL = 500 Ohm
VIL = 0 V; VIH = 4.5 V

Parameter	Symbol	min.	typ.	max.	Unit
A, B --> Y	tPLH		8	21	ns
A, B --> Y	tPHL		11	21	ns
S --> Y1)	tPLH		20	32	ns
S --> Y1)	tPHL		18	25	ns
OE --> Y	tPZH		10.5	25	ns
OE --> Y	tPZL		13.5	30	ns
OE --> Y	tPHZ		8.5	26	ns
OE --> Y	tPLZ		13	30	ns

1) Set data inputs A to L level, data inputs B to H level

Low-Power Schottky TTL Circuits (LS-TTL)

The Low-Power Schottky TTL (LS-TTL) circuits exhibit a power consumption lower by a factor of 5 compared to standard TTL circuits, at the same delay time.

This results in the following advantages for the user:
- Reduction of power dissipation at constant packing density,
- Increased reliability,
- Smaller power supply modules,
- Lower current density and thus less interference.

The LS-TTL series is compatible with other circuits of the TTL family and the HCT-CMOS series.

Absolute Maximum Ratings

Parameter	Symbol	min.	max.	Unit
Supply voltage	VCC	0	7	V
Input voltage	VI	-0.5	7	V
Output voltage (active)	VO		VCC+0.5	V
Output voltage (Tristate)	VOZ		5.5	V
Operating temperature range	Ta	0	70	degC
Junction temperature	Tj		150	degC

Selected Characteristics LS-TTL ICs

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Supply voltage	VCC		4.75	5.0	5.25	V
High input voltage	VIH		2.0			V
Low input voltage	VIL				0.8	V
Input clamp voltage	-VIK	VCC=4.75V, -II=18mA		0.9	1.5	V
High output current	-IOH				400	uA
Low output current	IOL				8	mA
High output voltage	VOH	VCC=4.75V, -IOH=400uA	2.7	3.3		V
Low output voltage	VOL	VCC=4.75V, IOL=8mA		0.35	0.5	V
Output leakage current (High)	IOZH	VCC=5.25V, VOH=2.4V			20	uA
Output leakage current (Low)	IOZL	VCC=5.25V, VOL=0.4V			20	uA
Input current (High)	IIH	VCC=5.25V, VIH=2.7V			20	uA
Input current (Low)	-IIL	VCC=5.25V, VIL=0.4V			360	uA
Input current	II	VCC=5.25V, VI=7V			100	uA
Short-circuit current	IOS	VCC=5.25V	20		100	mA

1) Not more than one output at a time, duration of short circuit < 1 sec

Package Dimensions

Figure 3: DIP-14, Plastic

Length: 19.5 max

Width: 6.7 max

Height: 4.5 (+0.5/-0.25)

Pin spacing: 2.54 mm (0.1 inch)

Pin width: 0.45 (+0.14/-0.1)

Pin thickness: 0.25 (+0.11/-0.05)

Figure 4: DIP-16, Plastic

Length: 19.5 max

Width: 6.7 max

Height: 4.5 (+0.5/-0.25)

Pin spacing: 2.54 mm (0.1 inch)

Pin width: 0.45 (+0.14/-0.1)

Pin thickness: 0.25 (+0.11/-0.05)

Figure 29: SO-16 (Small Outline)

Body length: 10.06 mm

Body width: 6.2 mm

Body height: 1.65 mm

Pin spacing: 1.27 mm

Pin width: 0.4 mm

Lead angle: 0...15 degrees

Flatness tolerance: 0.15

Pin position tolerance: T/2 = 0.125

Figure 30: SO-20 (Small Outline)

Body length: 12.85 mm

Body width: 10.4 (+0.5) mm

Body height: 2.5 mm

Pin spacing: 1.27 mm

Pin width: 0.4 mm

Lead angle: 90 (+/-10) degrees

Flatness tolerance: 0.15

Pin position tolerance: T/2 = 0.125