3 1/2 Digit, LED Display, A/D Converters

General Description

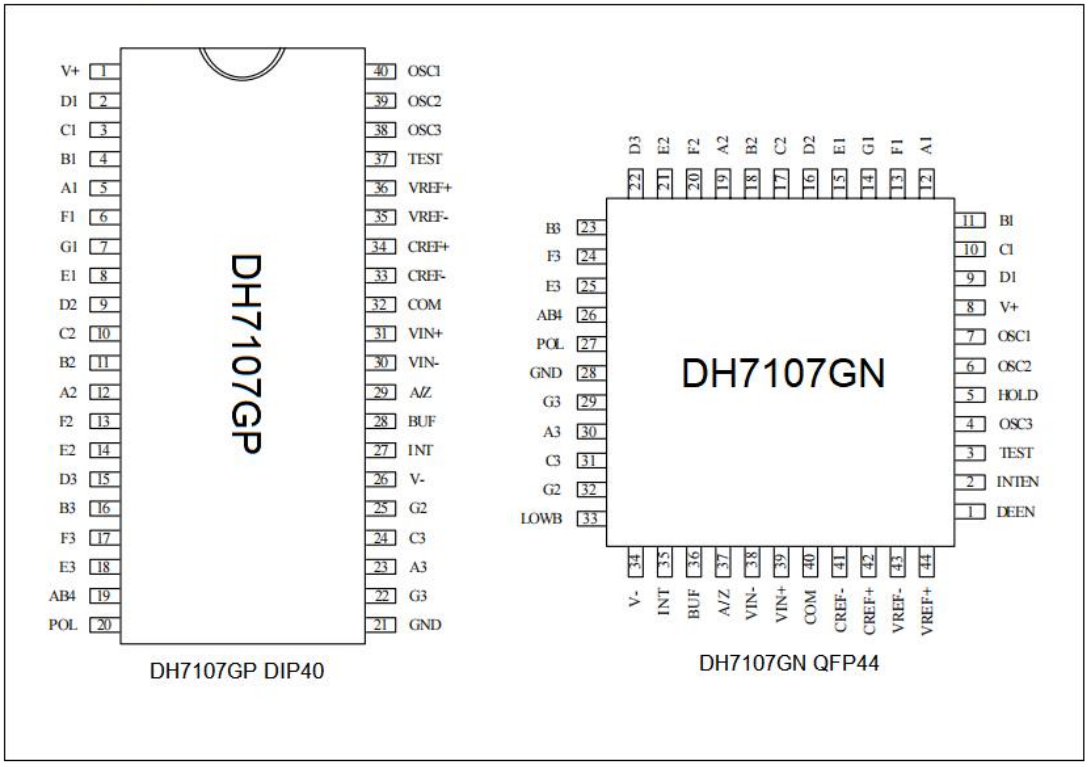
The DH7107 are high performance, low power, 3 1/2 digit A/D converters. Included are seven segment decoders, display drivers, a reference, and a clock. The DH7107 will directly drive an instrument size light emitting diode (LED) display.

The DH7107 bring together a combination of high accuracy, versatility, and true economy. It features auto-zero to less than 10μV, zero drift of less than 1μV/℃, input bias current of 10pA (Max), and rollover error of less than one count. True differential inputs and reference are useful in all systems, but give the designer an uncommon advantage when measuring load cells, strain gauges and other bridge type transducers.

Features

- Guaranteed Zero Reading for 0V Input on All Scales
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- True Differential Input and Reference, Direct Display Drive - LED DH7107
- Low Noise - Less Than 15μV_{P-P}
- On Chip Clock and Reference
- Low Power Dissipation - Typically Less Than 10mW
- No Additional Active Circuits Required
- Enhanced Display Stability
- Package: DIP40(DH7107GP)、QFP44(DH7107GN)

Pin Configuration



Analog Block Diagram

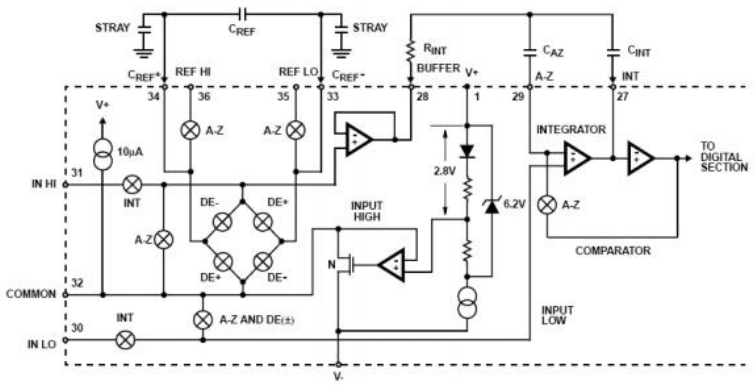


Figure 1

Functional Description

Analog Section

Figure 1 shows the Analog Section for the DH7107. Each measurement cycle is divided into three phases.

They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

Signal Integrate Phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range: up to 1V from either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

De-Integrate Phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is:

$$\text{DISPLAY COUNT} = 1000\left[\frac{V_{IN}}{V_{REF}}\right]$$

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 0.5V below the positive supply to 1V above the negative supply. In this range, the system has a CMRR of 86dB typical. However, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up
by the positive common mode voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3V of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for positive or negative input voltage will give a roll-over error. However, by selecting the reference capacitor such that it is large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count worst case.

Analog COMMON

This pin is included primarily to set the common mode voltage for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (0.001%/V), low output impedance (≦15Ω), and a temperature coefficient typically less than 80ppm/℃.

The limitations of the on chip reference should also be recognized, however. With the DH7107, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25μV to 80μV$_{P-P}$. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111(8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an over-range condition. This is because over-range is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between over-range and a non-over-range count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently tied to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N-Channel FET that can sink approximately 30mA of current to hold the voltage 2.8V below the positive supply (when a load is trying to pull the common line positive).

However, there is only 10μA of source current, so COMMON may easily be tied to a more negative voltage thus overriding the internal reference.

Digital Section

Figure 2 is the Digital Section of the DH7107.

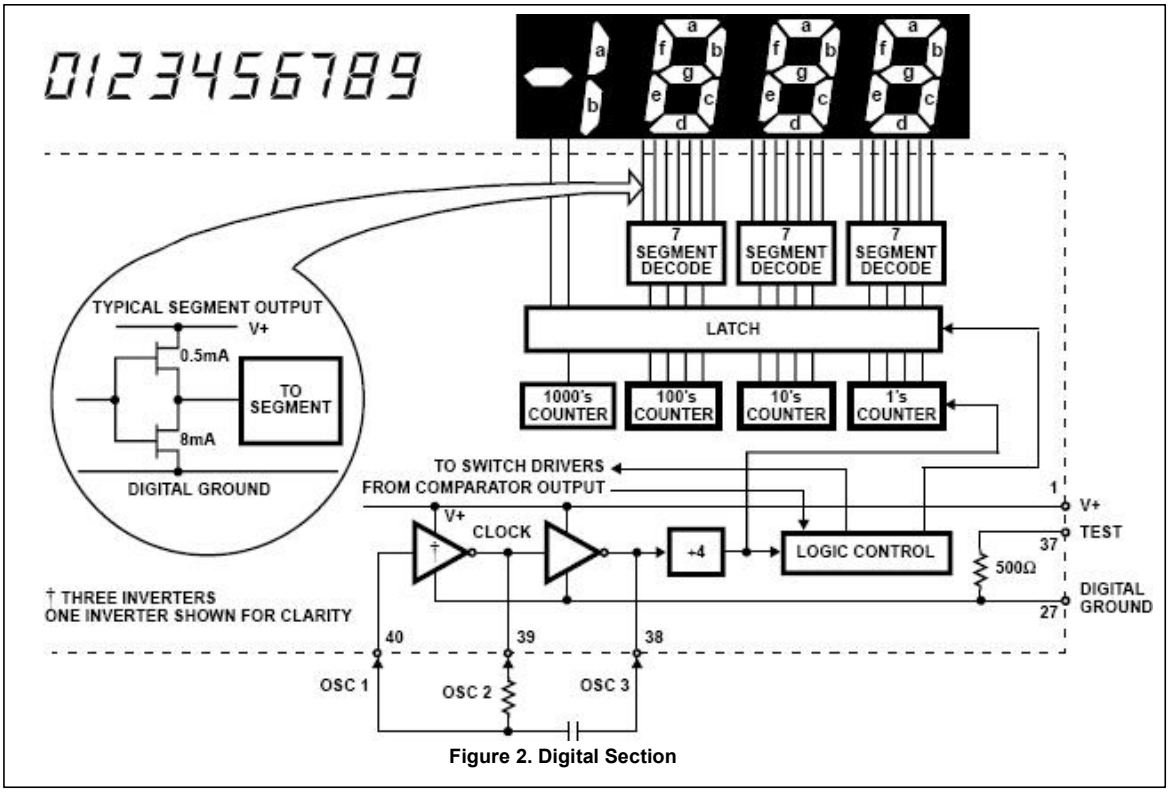


Figure 2. Digital Section

System Timing

Figure 3 shows the clocking arrangement used in the DH7107. Two basic clocking arrangements can be used:

1. Figure 3A. An external oscillator connected to pin 40.
2. Figure 3B. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 counts (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, $33^{1}/3$kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, $66^{2}/3$kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40k

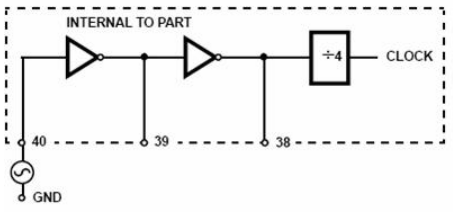


Figure 3A

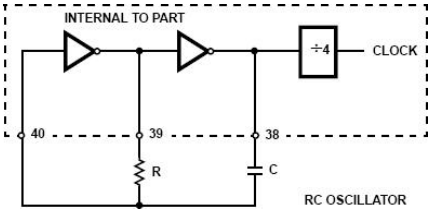


Figure 3B

Figure 3. Clock Circuits

Component Value Selection

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current.

They can supply 4μA of drive current with negligible nonlinearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full scale, 470kΩ is near optimum and similarly a 47kΩ for a 200mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance buildup will not saturate the integrator swing(approximately. 0.3V from either supply). When the analog COMMON is used as a reference, a nominal +2V fullscale integrator swing is fine. For the DH7107 with +5V supplies and analog COMMON tied to supply ground, a ±3.5V to +4V swing is nominal. For three readings/second(48kHz clock) nominal values for CINT are 0.22μF and 0.10μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is thatit must have a low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.47μF capacitor is recommended. On the 2V scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e., the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1mF will hold the roll-over e

Oscillator Components

For all ranges of frequency a 100kΩ resistor is recommended and the capacitor is selected from the equation:

f= 0.45/RC For 48kHz Clock (3 Readings/sec), c=100pF

Reference Voltage

The analog input required to generate full scale output (2000 counts) is: VIN = 2VREF. Thus, for the 200mV and 2V scale, VREF should equal 100mV and 1V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.662V. Instead of dividing the input down to 200mV, the designer should use the input voltage directly and select VREF = 0.341V. Suitable values for integrating resistor and capacitor would be 1 20kΩ and 0.22μF. This makes the system slightly quieter and also avoids a divider network on the input. The DH7107 with ±5V supplies can accept input signals up to ±4V. Another advantage of this system occurs when a digital reading of zero is desired for VIN ≠0. Temperature and weighing systems with a variable fare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

Power Supplies

The DH7107 is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive IC. Figure 4 shows this application.

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5V.
3. An external reference is used.

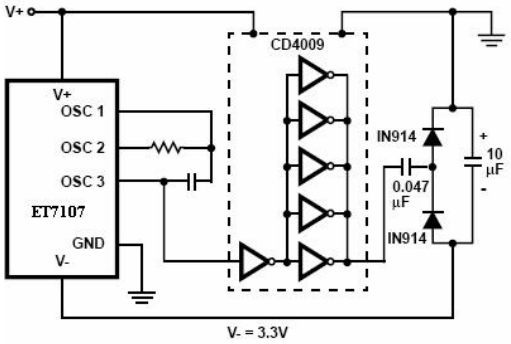


Figure 4. Generating Negative Supply from +5V

Design Information Summary Sheet

- **OSCILLATOR FREQUENCY**

f_{osc} = 0.45/RC

C_{OSC} > 50pF; ROSC > 50kΩ

f_{osc}(Typ) = 48kHz

- **OSCILLATOR PERIOD**

t_{OSC} = RC/0.45

- **INTEGRATION CLOCK FREQUENCY**

f_{CLOCK} = fOSC/4

- **INTEGRATION PERIOD**

t_{INT} = 1000 x (4/fOSC)

- **60/50Hz REJECTION CRITERION**

t_{INT}/t60Hz or t_{INT}/t60Hz = Integer

- **OPTIMUM INTEGRATION CURRENT**

I_{INT} = 4µA

- **FULL SCALE ANALOG INPUT VOLTAGE**

V_{INFS} (Typ) = 200mV or 2V

- **INTEGRATE RESISTOR**

$$R_{INT} = \frac{V_{INFS}}{I_{INT}}$$

- **INTEGRATE CAPACITOR**

$$C_{INT}=\frac{(t_{INT})(I_{INT})}{V_{INT}}$$

- **INTEGRATOR OUTPUT VOLTAGE SWING**

$$V_{INT}=\frac{(t_{INT})(I_{INT})}{C_{INT}}$$

- **VINT MAXIMUM SWING:**

(V- + 0.5V) < VINT < (V+ - 0.5V), VINT (Typ) = 2V

DISPLAY COUNT

$$COUNT=1000*\frac{V_{IN}}{V_{REF}}$$

- **CONVERSION CYCLE**

$t_{CYC} = t_{CLOCK}$ x 4000 $t_{CYC} = t_{OSC}$ x 16,000

when f_{OSC} = 48kHz; t_{CYC} = 333ms

- **COMMON MODE INPUT VOLTAGE**

(V- + 1V) < VIN < (V+ - 0.5V)

- **AUTO-ZERO CAPACITOR**

0.01μF < CAZ < 1μF

- **REFERENCE CAPACITOR**

0.1μF < CREF < 1μF

- **V_{COM}**

Biased between Vi and V-.

- **V_{COM} ≦ V+ - 2.8V**

Regulation lost when V+ to V- < ≦6.8V

If VC_{OM} is externally pulled down to (V+ to V-)/2, the V_{COM} circuit will turn off.

- **POWER SUPPLY: DUAL ±5.0V**

V+ = +5V to GND

V- = -5V to GND

Digital Logic and LED driver supply V+ to GND

- **DISPLAY: LED**

Type: Non-Multiplexed Common Anode

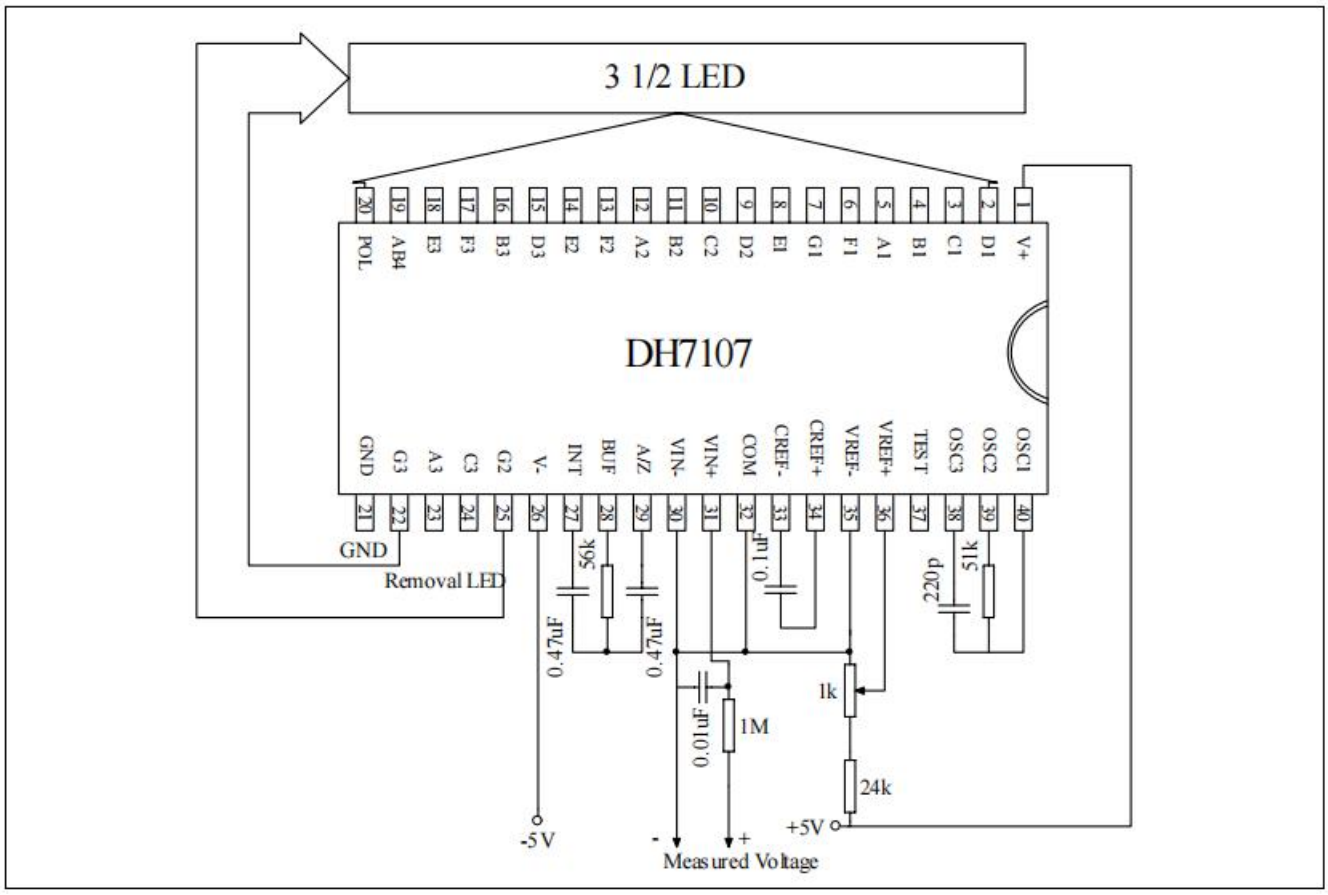
Absolute Maximum Ratings

Parameter	Ratings	Unit
V+ to GND	6	V
V- to GND	-6	V
Analog Input Voltage(Either Input)	V+ to V-	
Reference Input Voltage(Either Input)	V+ to V-	
Clock Input	GND to V+	
Power Dissipation	800	mW
Working Temperature	-25～70	℃
Storage Temperature	-25～100	℃
Maximum Lead Temperature(Soldering 60s)	300	℃

Electrical Characteristics

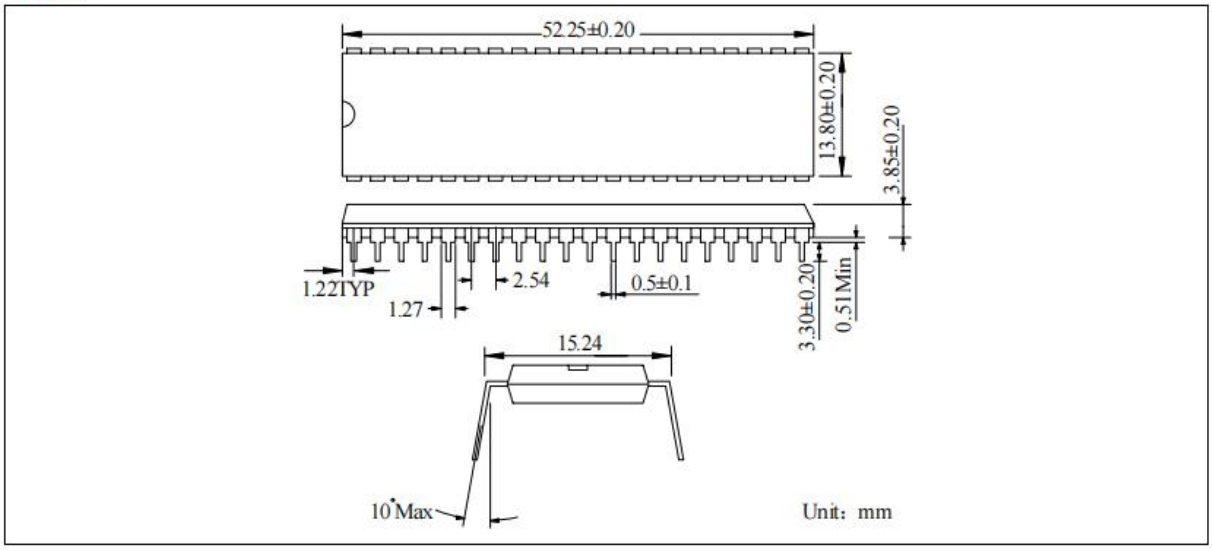
Parameter	Test Condition	Min.	Typ.	Max.	Unit
Zero Input Reading	V_{IN}=0.0V, Full Scale=200mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	V_{IN}=V_{REF}，V_{REF}=100mV	999	999/1000	1000	Digital Reading
Rollover Error	-V_{IN}=+V_{IN}=200mV	-1	±0.2	+1	counts
Linearity	Full Scale=200mV or 2.000V	-1	±0.2	+1	counts
Common Mode Rejection Ratio	V_{CM}=±1V, V_{IN}=0V, Full Scale=200.0mV	—	50	—	μV/V
Noise	V_{IN}=0V, Full Scale=200.0mV	—	15	—	μV
Leakage Current Input	V_{IN}=0V	—	1	10	pA
Zero Reading Drift	V_{IN}=0V	—	0.2	1	μV/℃
Scale Factor Temperature Coefficient	V_{IN}=199.0mV	—	1	5	ppm/℃
End Power Supply Character V+ Supply Current	V_{IN}=0V	—	0.8	1.8	mA
Common Pin Analog Common Voltage	25kΩ Between Common and Positive Supply	2.7	3.05	3.35	V
Temperature Coefficient of Analog Common(With Respect to + Supply)	25kΩ Between Common and Positive Supply	—	20	50	ppm/℃
Temperature Coefficient of Analog Common(With Respect to - Supply)	25kΩ Between Common and Positive Supply	—	—	75	ppm/℃
Segment Sinking Current	+V=5.0V, Segment Voltage=3V	5	8.0	—	mA
Segment Sinking Current，Pin19	+V=5.0V, Segment Voltage=3V	10	16	—	mA
Segment Sinking Current，Pin20	+V=5.0V, Segment Voltage=3V	4	7	—	mA

Application Circuits



Package Dimension

DIP40



QFP44