

MOSFET – N-Channel, POWERTRENCH®

100 V, 74 A, 12 mΩ

FDP120N10

Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

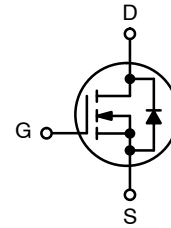
Features

- $R_{DS(on)} = 9.7 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 74 \text{ A}$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability RoHS Compliant
- This Device is Pb-Free, Halide Free and RoHS Compliant

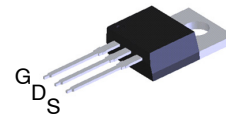
Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micor Solar Inverter

V_{DS}	$R_{DS(on)}$ TYP	I_D MAX
100 V	9.7 mΩ @ 10 V	74 A

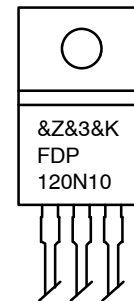


N-Channel MOSFET



TO-220-3LD
CASE 340AT

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= 3-Digit Date Code Format
&K	= 3-Digit Lot Run Traceability Code
FDP120N10	= Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
FDP120N10	TO-220 (Pb-Free)	800 Units / Tube

FDP120N10

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		FDP120N10	Unit
V_{DSS}	Drain to Source Voltage		100	V
V_{GSS}	Gate to Source Voltage		± 20	V
I_D	Drain Current	– Continuous ($T_C = 25^\circ\text{C}$, Silicon Limited)	74	A
		– Continuous ($T_C = 100^\circ\text{C}$, Silicon Limited)	52	
I_{DM}	Drain Current	– Pulsed (Note 1)	296	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		198	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		6.0	V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	170	W
		– Derate Above 25°C	1.14	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to $+175$	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $L = 0.11 \text{ mH}$, $I_{AS} = 60 \text{ A}$, $V_{DD} = 50 \text{ V}$, $R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 74 \text{ A}$, $di/dt \leq 200 \text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDP120N10	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.88	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

FDP120N10

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$, $T_C = 25^\circ\text{C}$	100	–	–	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	–	0.1	–	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100\ \text{V}$, $V_{GS} = 0\ \text{V}$	–	–	1	μA
		$V_{DS} = 100\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_C = 150^\circ\text{C}$	–	–	500	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	2.5	–	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 74\ \text{A}$	–	9.7	12	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10\ \text{V}$, $I_D = 74\ \text{A}$	–	105	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 25\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	–	4215	5605	pF
C_{oss}	Output Capacitance		–	405	540	pF
C_{rss}	Reverse Transfer Capacitance		–	170	255	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{DS} = 80\ \text{V}$, $I_D = 74\ \text{A}$, $V_{GS} = 10\ \text{V}$ (Note 4)	–	66	86	nC
Q_{gs}	Gate to Source Gate Charge		–	26	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	20	–	nC

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\ \text{V}$, $I_D = 74\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_G = 4.7\ \Omega$ (Note 4)	–	27	64	ns
t_r	Turn-On Rise Time		–	105	220	ns
$t_{d(off)}$	Turn-Off Delay Time		–	39	88	ns
t_f	Turn-Off Fall Time		–	15	40	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	74	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	296	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_{SD} = 74\ \text{A}$	–	–	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\ \text{V}$, $I_{SD} = 74\ \text{A}$, $di_F/dt = 100\ \text{A}/\mu\text{s}$	–	44	–	ns
Q_{rr}	Reverse Recovery Charge		–	67	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Package limitation current is 120 A.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

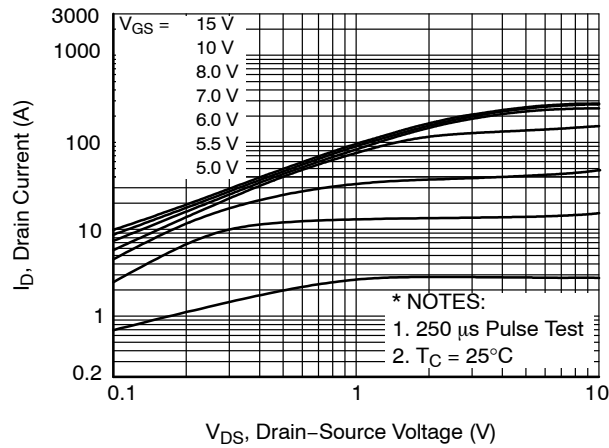


Figure 1. On-Region Characteristics

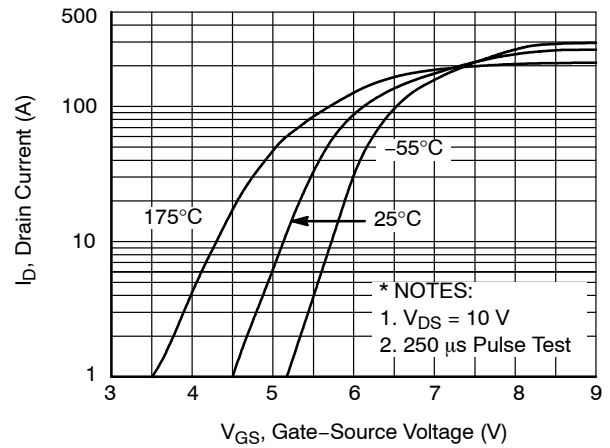


Figure 2. Transfer Characteristics

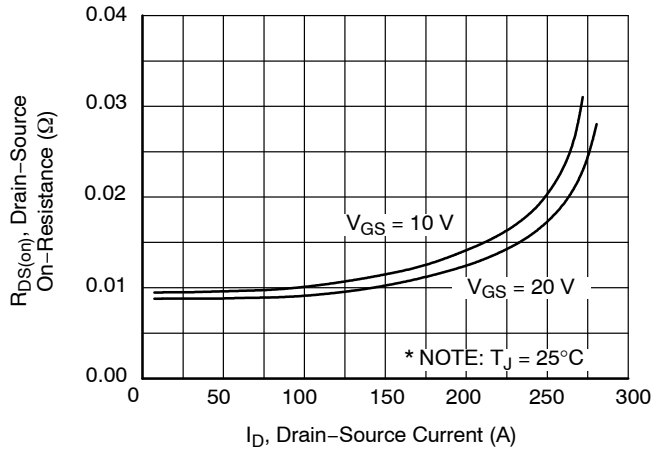


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

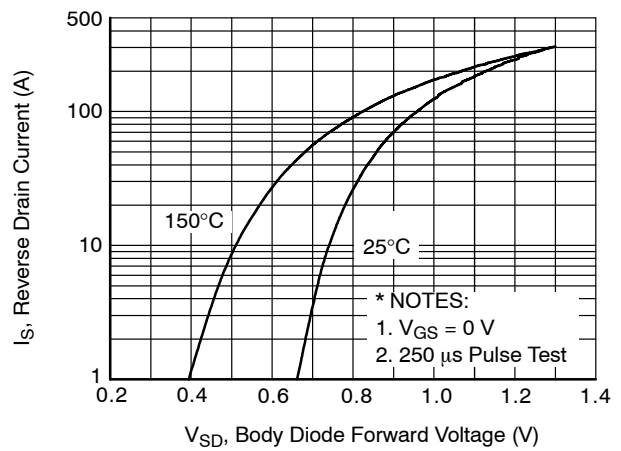


Figure 4. Body Diode Forward Voltage Variation vs. Source Current And Temperature

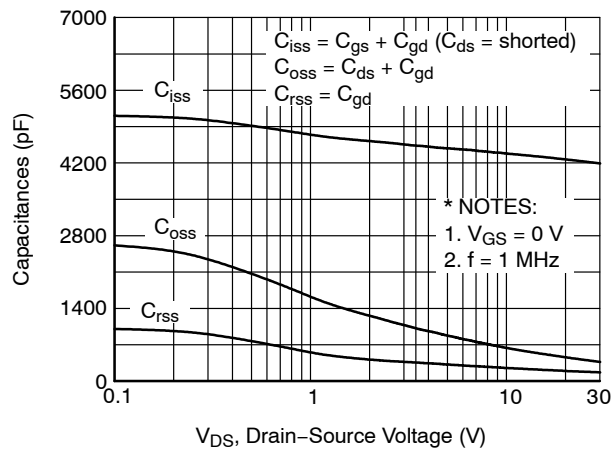


Figure 5. Capacitance Characteristics

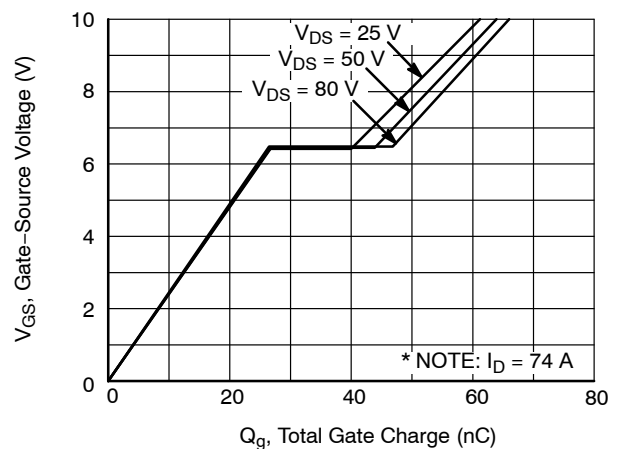


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

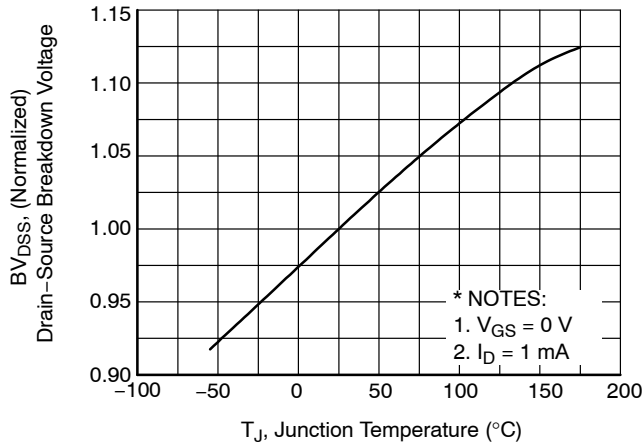


Figure 7. Breakdown Voltage Variation vs. Temperature

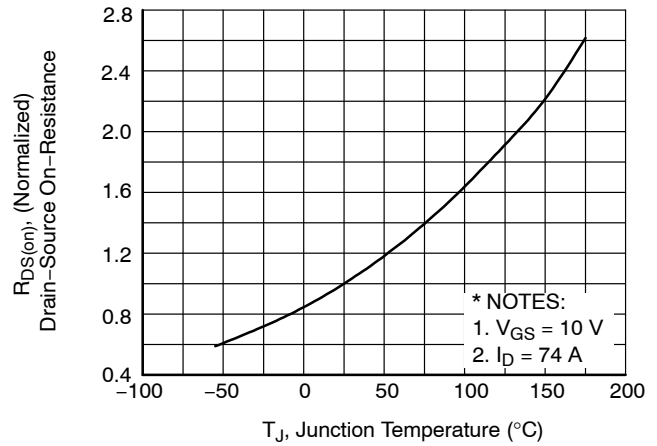


Figure 8. On-Resistance Variation vs. Temperature

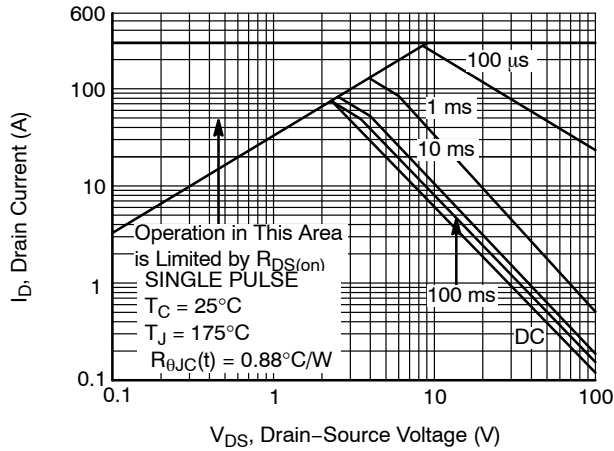


Figure 9. Maximum Safe Operating Area

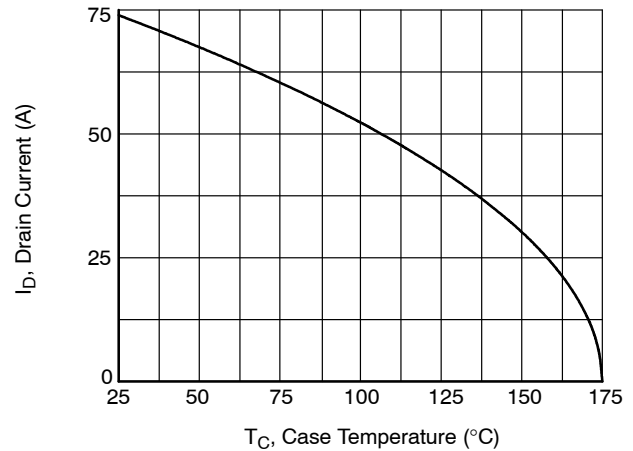


Figure 10. Maximum Drain Current vs. Case Temperature

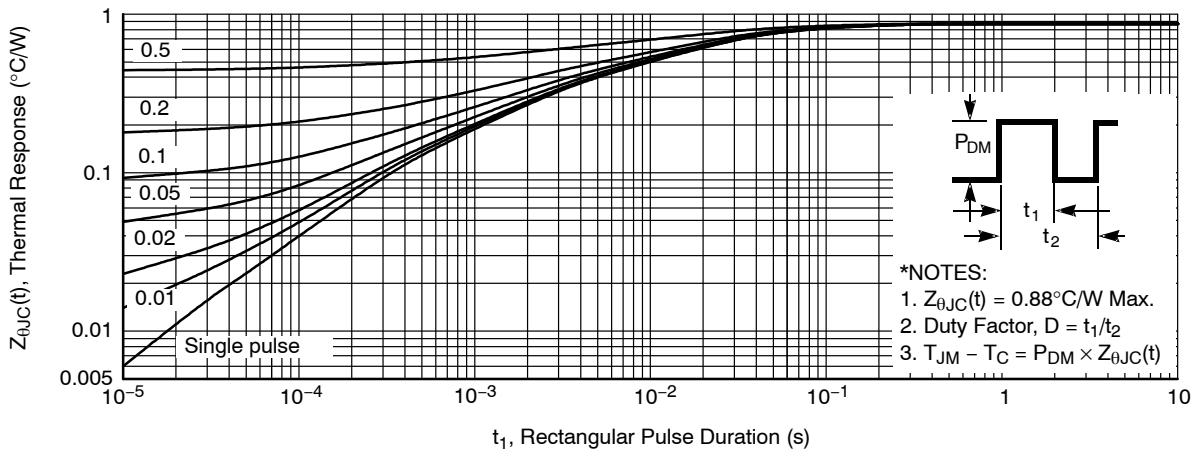


Figure 11. Transient Thermal Response Curve

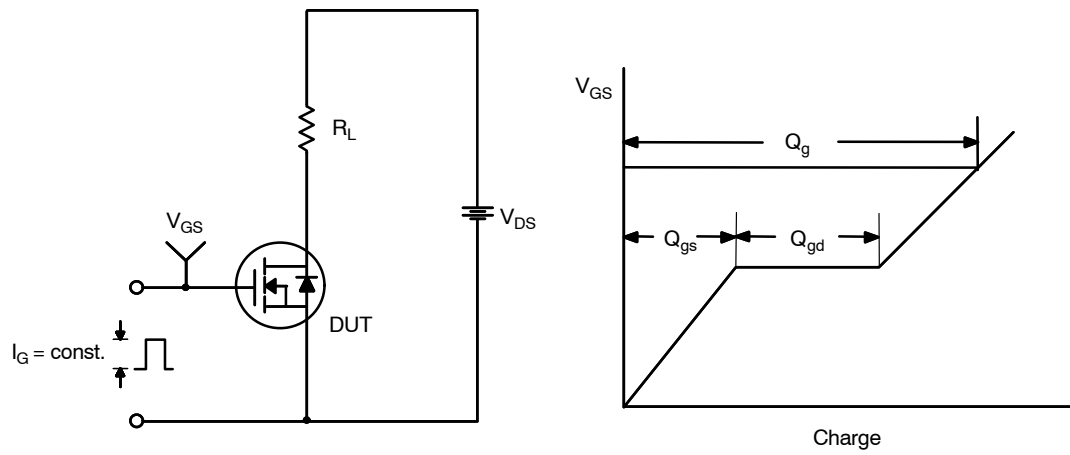


Figure 12. Gate Charge Test Circuit & Waveform

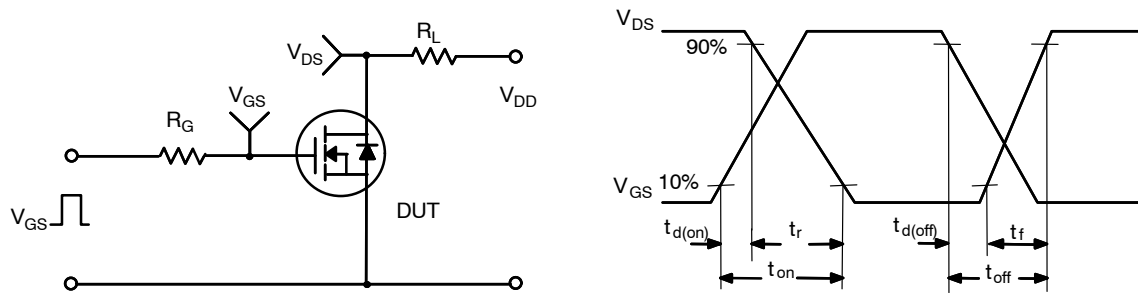


Figure 13. Resistive Switching Test Circuit & Waveforms

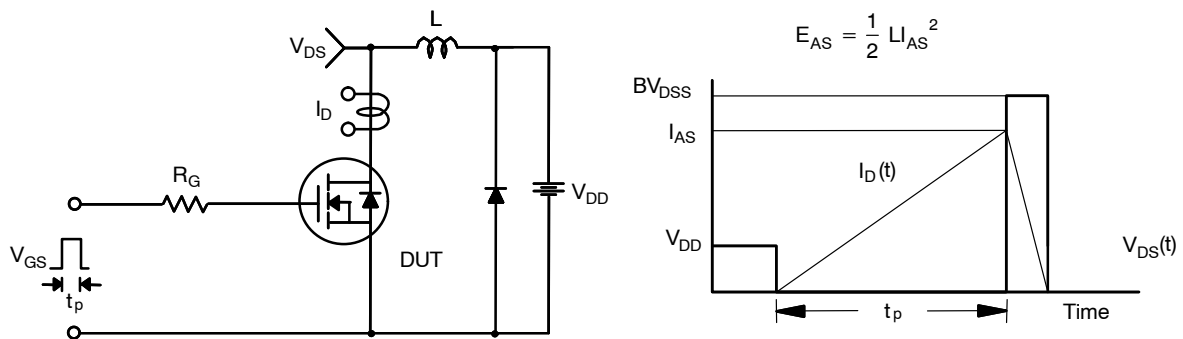


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

FDP120N10

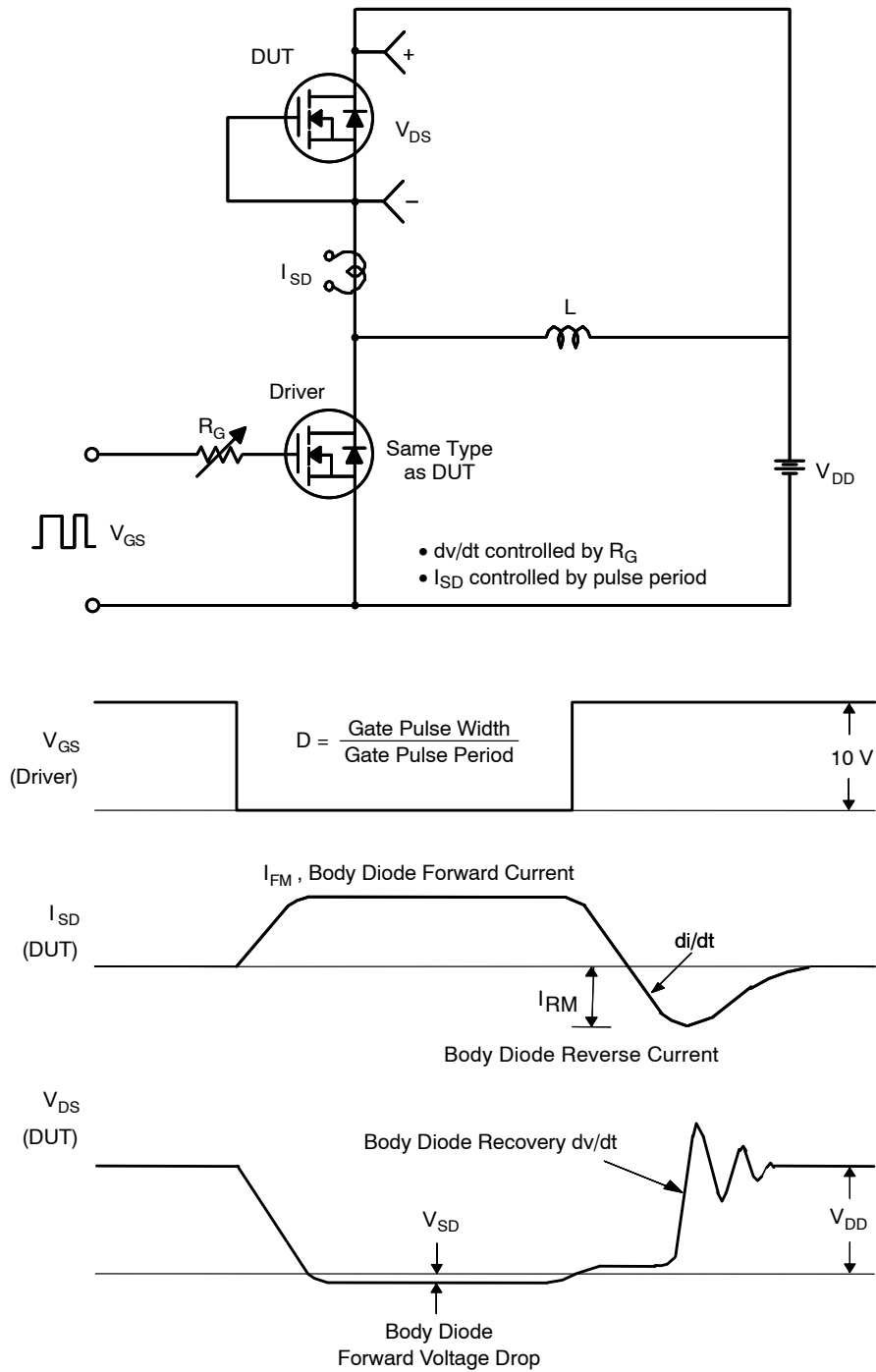
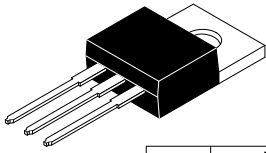


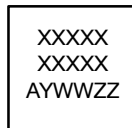
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms


TO-220-3LD
CASE 340AT
ISSUE B

DATE 08 AUG 2022

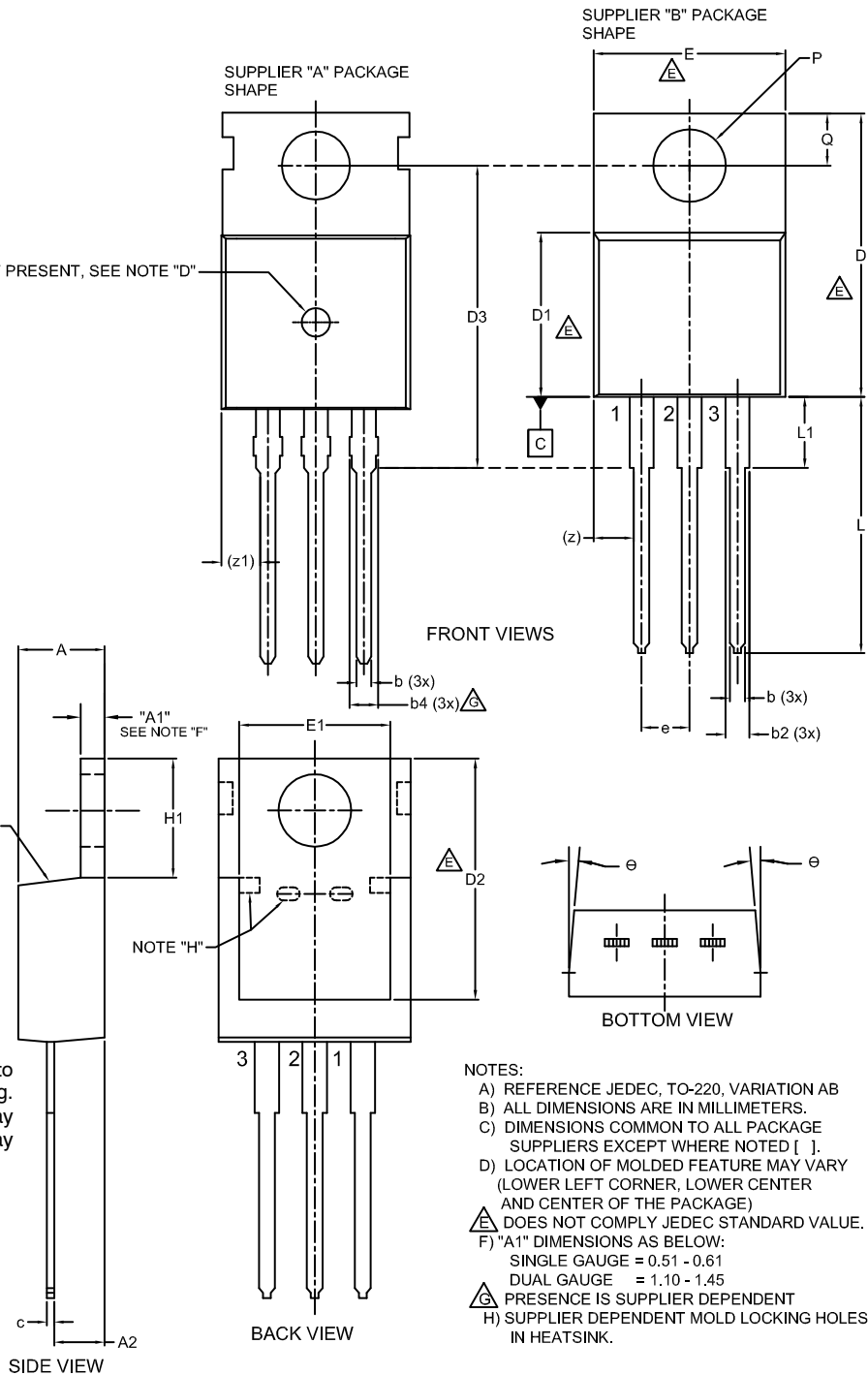
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.00	--	4.70
A1	SEE NOTE "F"		
A2	2.10	--	2.85
b	0.55	--	1.00
b2	1.10	--	1.62
b4	1.42	--	1.62
c	0.36	--	0.60
D	13.90	--	16.30
D1	8.13	--	9.40
D2	11.50	--	14.30
D3	15.42	--	16.51
E	9.65	--	10.67
E1	7.59	--	8.65
e	2.40	--	2.67
H1	6.06	--	6.69
L	12.70	--	14.04
L1	2.70	--	4.10
P	3.50	--	4.00
Q	2.50	--	3.40
z	2.13 REF		
z1	2.06 REF		
θ	3°	--	5°

IF PRESENT, SEE NOTE "D"

GENERIC
MARKING DIAGRAM*


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



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