2SK2800

Silicon N Channel MOS FET
High Speed Power Switching

HITACHI

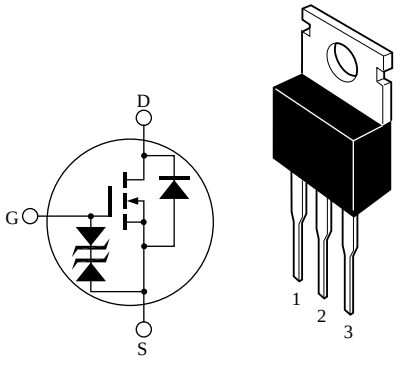
ADE-208-513G (Z)
8th. Edition
Jun 1998

Features

- Low on-resistance
  $R_{DS(on)}$ = 15 mΩ typ.
- High speed switching
- Low drive current
- 4V gate drive device can be driven from 5V source

Outline

TO–220AB



1. Gate
2. Drain (Flange)
3. Source

Hitachi semiconductor

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	40	A
Drain peak current	$I_{D(pulse)}$ Note1	160	A
Body-drain diode reverse drain current	I_{DR}	40	A
Avalanche current	I_{AP} Note 3	40	A
Avalanche energy	E_{AR} Note 3	137	mJ
Channel dissipation	Pch Note 2	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Note: 1. PW ≤ 10μs, duty cycle ≤ 1 %
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50Ω

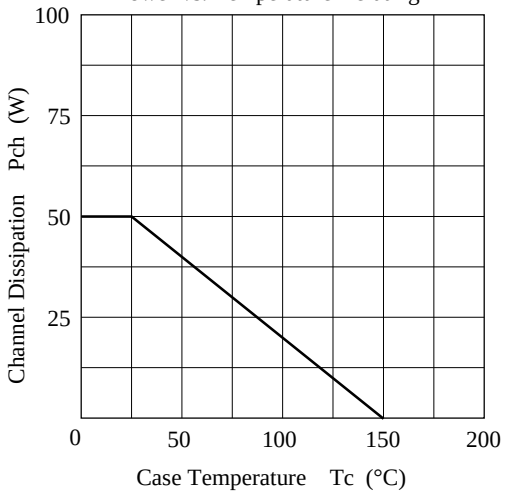
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16V, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	10	µA	V_{DS} = 60 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	2.5	V	I_D = 1mA, V_{DS} = 10V
Static drain to source on state resistance	$R_{DS(on)}$	—	15	20	mΩ	I_D = 20A, V_{GS} = 10V [Note4]
	$R_{DS(on)}$	—	25	40	mΩ	I_D = 20A, V_{GS} = 4V [Note4]
Forward transfer admittance	$\|y_{fs}\|$	20	35	—	S	I_D = 20A, V_{DS} = 10V [Note4]
Input capacitance	Ciss	—	1500	—	pF	V_{DS} = 10V
Output capacitance	Coss	—	720	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	200	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 20A, R_L = 1.5Ω
Rise time	t_r	—	180	—	ns	V_{GS} = 10V
Turn-off delay time	$t_{d(off)}$	—	200	—	ns	
Fall time	t_f	—	200	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.95	—	V	I_F = 40A, VGS = 0
Body–drain diode reverse recovery time	t_{rr}	—	70	—	V	I_F = 40A, VGS = 0 diF/ dt =50A/µs

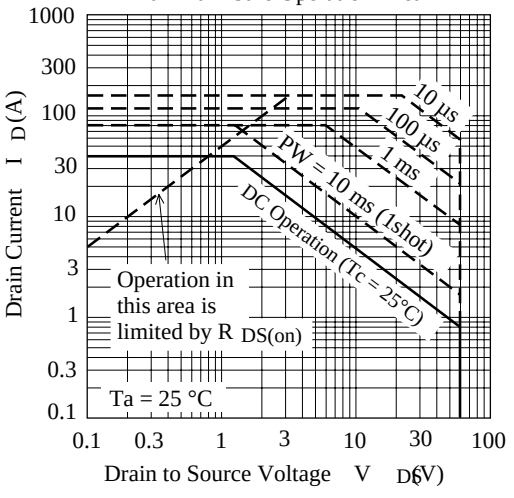
Note: 4. Pulse test

Main Characteristics

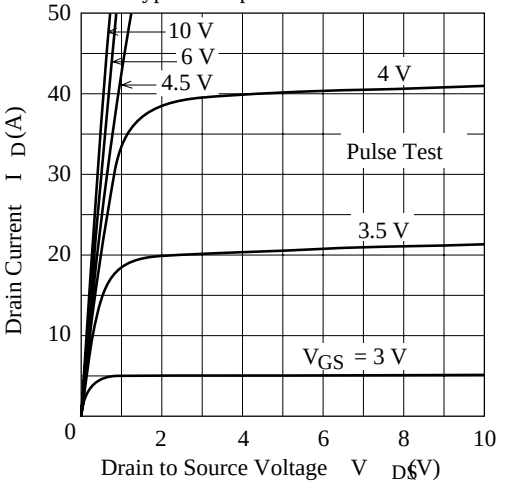
Power vs. Temperature Derating



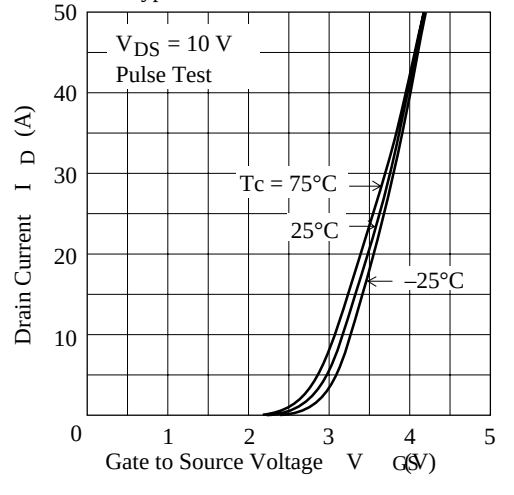
Maximum Safe Operation Area



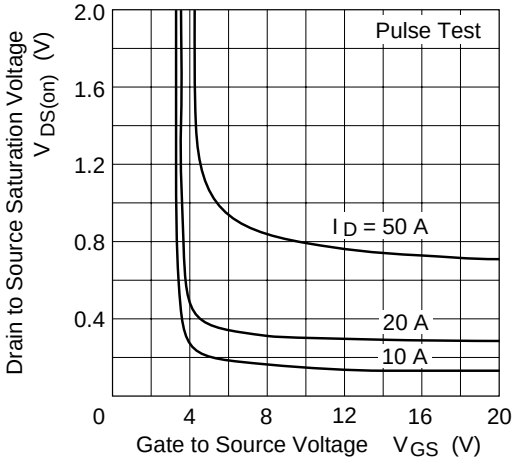
Typical Output Characteristics



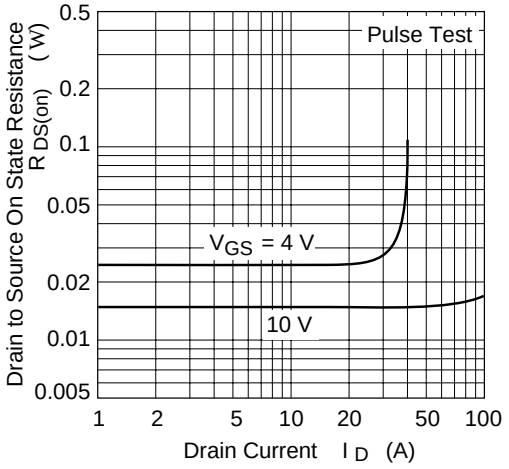
Typical Transfer Characteristics



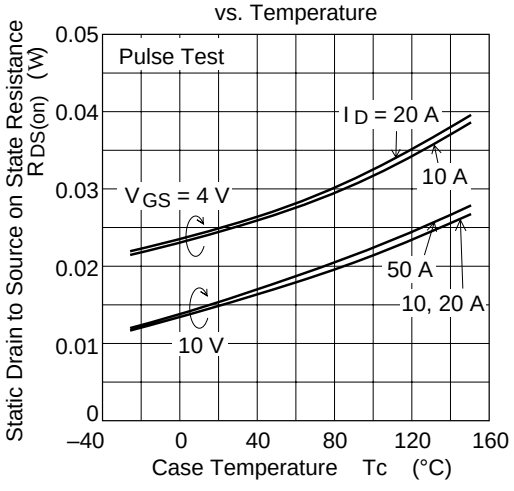
Drain to Source Saturation Voltage vs. Gate to Source Voltage



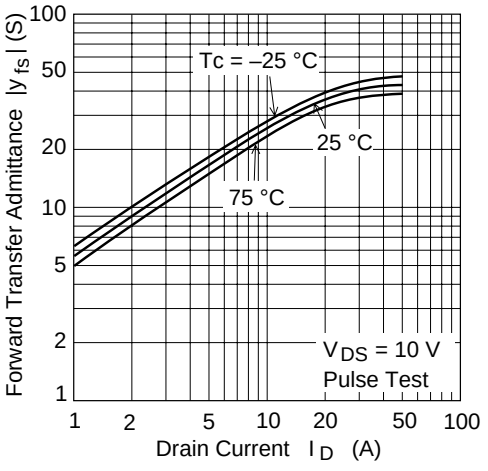
Static Drain to Source on State Resistance vs. Drain Current



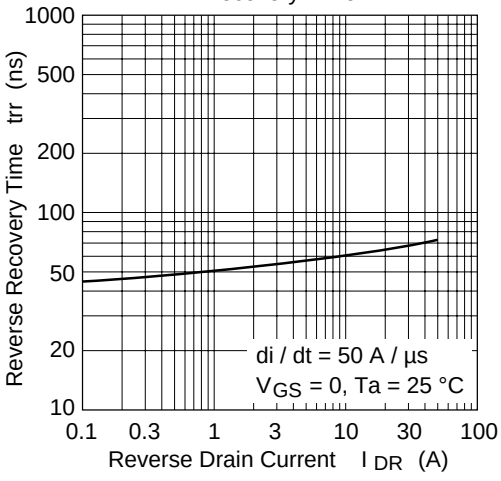
Static Drain to Source on State Resistance vs. Temperature



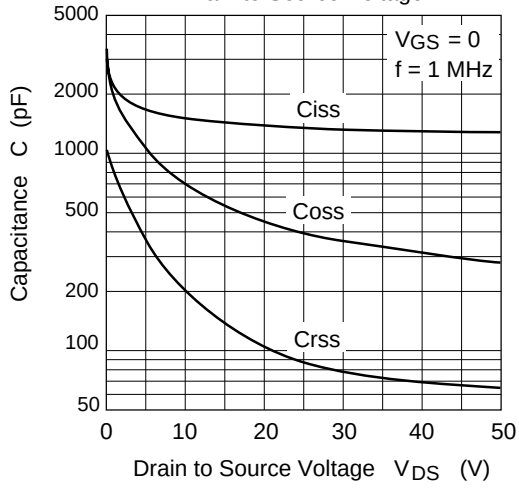
Forward Transfer Admittance vs. Drain Current



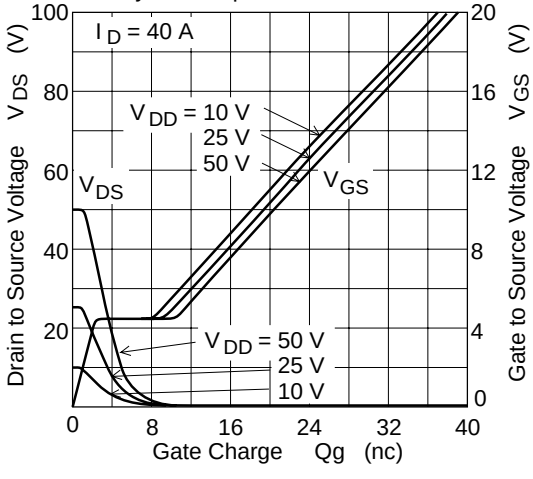
Body–Drain Diode Reverse Recovery Time



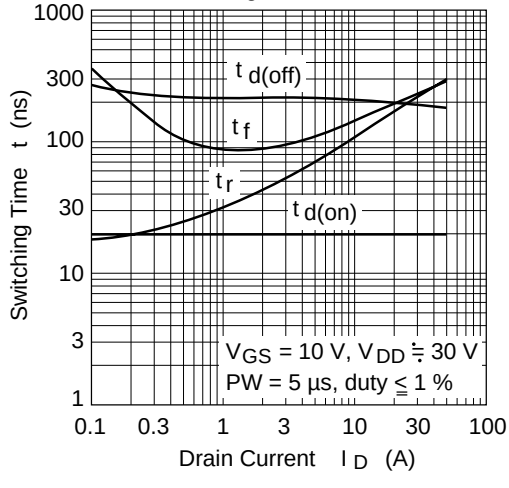
Typical Capacitance vs. Drain to Source Voltage



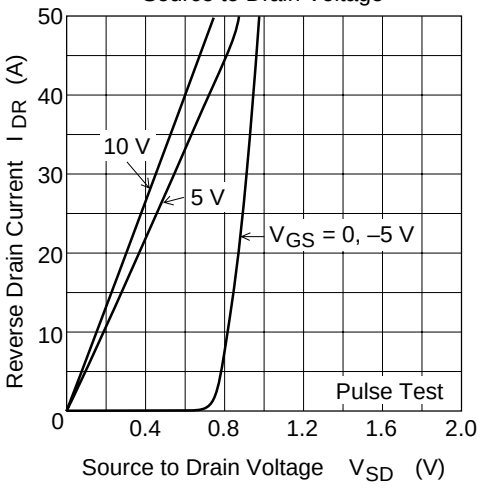
Dynamic Input Characteristics



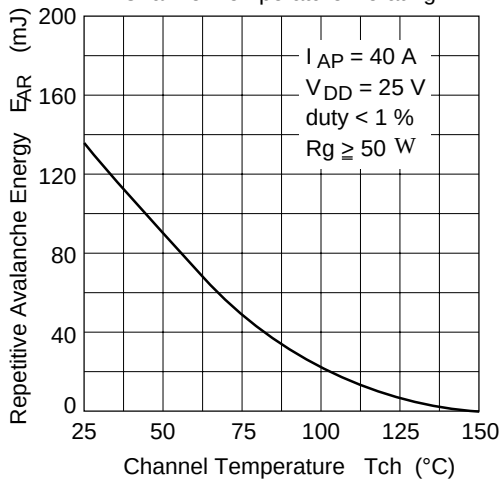
Switching Characteristics



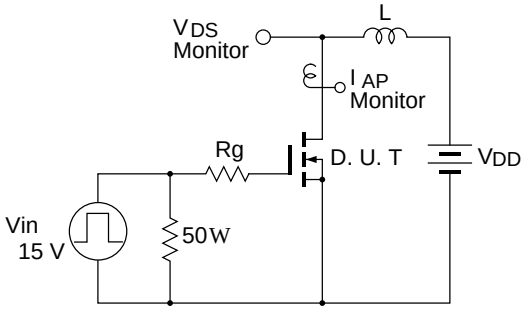
Reverse Drain Current vs.
Source to Drain Voltage



Maximum Avalanche Energy vs.
Channel Temperature Derating

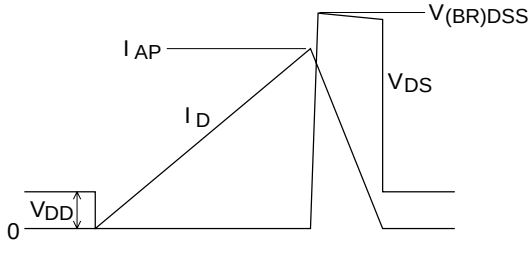


Avalanche Test Circuit

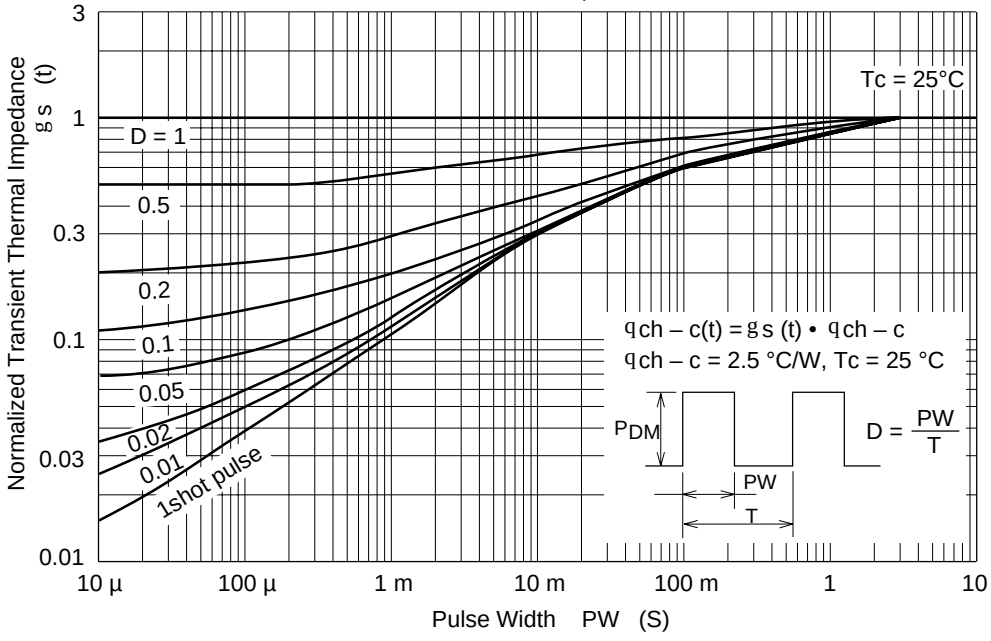


Avalanche Waveform

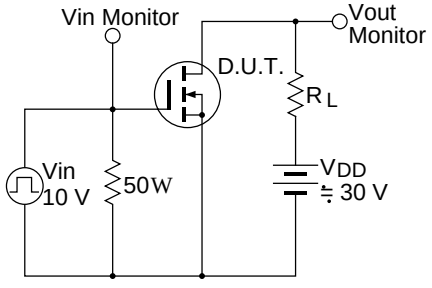
$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}^{2} \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



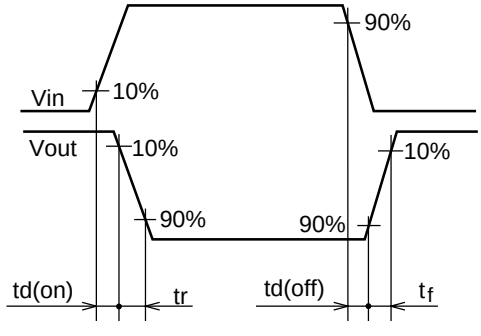
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

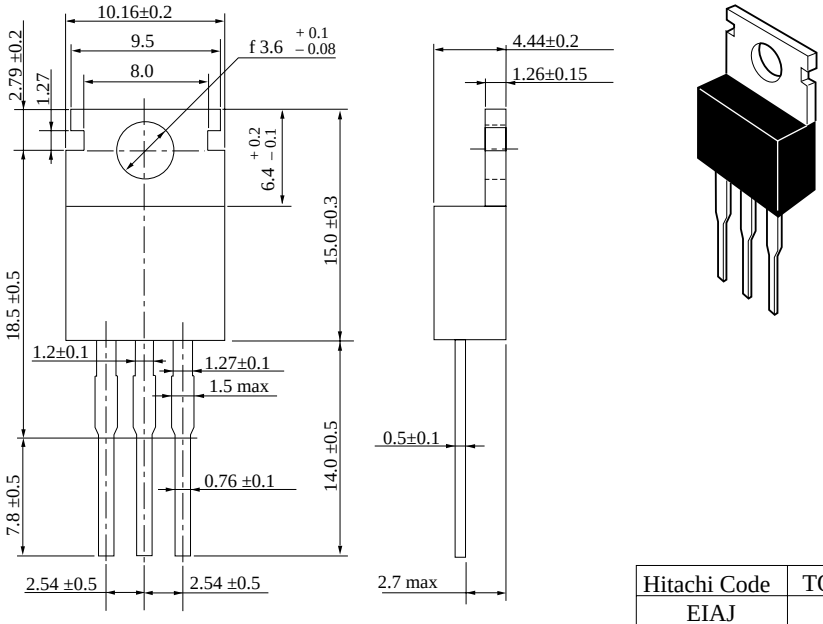


Waveform



Package Dimensions

Unit: mm



Hitachi Code	TO–220AB
EIAJ	SC–46
JEDEC	—

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